PERFORMANCE EVALUATION OF TRANSISTOR CLAMPED H-BRIDGE (TCHB) BASED FIVE-LEVEL MULTILEVEL INVERTER TOPOLOGIES

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Abstract: Multilevel inverters are suitable for various high voltage and high-power applications due to their ability to synthesize waveforms with better harmonic spectrum and steady output. Lower output harmonics and lower commutation losses make the multilevel converters capable of handling high power applications. Their fundamental drawback is complex circuitry, obliging a high number of power devices and passive components. So, a topology called Transistor Clamped H-Bridge Multilevel Inverter (TCHB) is proposed to generate a 5 Level output voltage with a reduced number of switches and to achieve even power distribution among the devices. But, reliability is a chief concern. Hence, in this project, the reliability improvement strategy for a newly developed five-level transistor clamped H-bridge-based multilevel inverter is simulated which can be generalised for any number of levels. In this strategy, the fault can be broadly classified based on the two main legs of the TCHB multilevel inverter. Moreover, this fault-tolerant strategy does not require any external circuit for maintaining its capacitor voltage in the balanced state. The Simulation results using Level shifted multicarrier modulation is presented & THD is observed. This topology reduces both the number of switches and the cost. From the results, this inverter provides higher output quality with relatively lower power loss as compared to the other conventional inverters with the same output quality. Also, a comparative study based on reliability and efficiency of a TCHB based five-level MLI using five switches and seven switches has been done, and the results have been tabulated.

Index Terms: Multilevel Inverter (MLI); TCHB five-level MLI; Reliability Improvement; THD; Efficiency.

I. INTRODUCTION

Recently by fast developing of high power devices and controlling methods, the multilevel inverter is becoming more popular in industrial companies. The Multilevel inverters are kind of power electronic devices which converts a DC voltage to favourable AC voltage [1]. Multilevel inverter (MLI) normally integrates the step voltage waveform from several levels of DC voltage sources. Power quality, less total harmonic distortion, reduced voltage stress across the switches, good electromagnetic compatibility, low switching losses and low dv/dr stress are the additional benefits of MLI [2]. Also, MLIs are effectively implemented in the field of AC motor drives [3, 4], active power filter [5, 6], integration of renewable energy sources [7, 8] and hybrid energy system [9, 10]. Essentially MLI is classified into three classes; they are neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB). In case higher number of output levels (>5), NPC and FC require complicated techniques for maintaining its capacitor voltage in the balanced state while CHB requires many isolated DC sources. Apart from the above problems, MLIs uses a high number of semiconductor devices which increase its cost and decrease the reliability.

According to a recently conducted industry-based survey on power converters, the semiconductor devices are the subtlest parts which result in low reliability of MLI as compared with two-level inverters [11,12]. Hence, the fault-tolerance is one of the major concerns in various industrial applications where continuity is most important, such as wind turbines and PV cells. Fault tolerance in MLIs can be achieved by adding redundant states along with the suitable reconfiguration of control strategy under faulty condition [13]. Redundancy can only be achieved by adding some devices in series/parallel in the conventional topologies.

Fault-tolerance is achieved by shorting the faulted switch and reconfiguring the control strategy. This topology uses additional SCR with each IGBT and pair of bidirectional switches in each leg which increases its cost. Topologies of [14,15,16,17] propose some modified topologies of NPC with two types of fault tolerant features, i.e., partial fault solution and complete fault solution. In partial fault solution, some levels get eliminated after the fault is reconfigured whereas, in case of complete fault solution, number of output levels is the same even after fault reconfiguration as that of the normal state. In all the modified topologies, the fourth leg of FC is added, which serves to keep the neutral point voltage oscillation as low as possible. The disadvantage of this topology is the inability to tolerate faults on its inner leg switches. Topology presented in [18] proposes fast fault detection technique for CHB based on the output voltage, frequency analysis; the fault is detected using an improved threshold level due to which faulty conditions and transient conditions are easily discriminated, but it cannot detect some open circuit faults which the limitation is. Fault detection and mitigation of CHB used in STATCOM for seven and eleven level inverter is proposed in [19,20] respectively.
In both the works, the faulted cell is bypassed with a suitable reconfiguration of the control strategy. It is to note here that the DC sources in the faulted cell remain unused which is the respective disadvantages.

This paper presents a new fault-tolerant technique for five-level transistor clamped H-bridge (TCHB) inverter which can be generalised for any number of levels by using cascading connections. TCHB inverter for symmetrical configuration was first proposed in [21]. It reduces the switch count and DC sources as compared with CHB and does not require any complicated circuits for maintaining its capacitor voltage in the balanced state. However, the main drawback of this topology is the loss of modularity. Hence, the cascaded version for symmetrical topology is proposed in [22] for symmetrical configuration to achieve the modularity in TCHB inverter. In [23], the asymmetrical operation of the TCHB inverter is proposed for high power quality applications. One of the major disadvantages of these inverters is the fault intolerance capabilities. Fault on switches of its H-bridge will lead to total shut down of the operation. Hence, in [24], the fault tolerance for TCHB topology is proposed, but for DC/DC converter. In this strategy, the third leg is added to the topology which operated in case of a fault. Therefore, the TCHB topologies lag in applications where continuity is utmost important as compared with CHB. Hence, in this paper, a new strategy for fault tolerance improvement of TCHB inverter is presented.

In this paper, five-level inverter topology that can tolerate faults on switches is presented. The fault on switches is classified based on the two main legs of the presented inverter. This topology is beneficial as it reduces the number of switches and isolated DC sources as compared with CHB and has an additional advantage of self-voltage balancing of its capacitor voltage even under post-fault conditions. Moreover, the proposed topology can be generalised for any number of levels by connecting the basic topology in a cascaded manner.

II. OPERATION AND PRINCIPLE OF THE TRANSISTOR CLAMPED H-BRIDGE (TCHB) FIVE-LEVEL MULTILEVEL INVERTER TOPOLOGIES:

2.1 Conventional Topology:

The figure below shows the new cascaded five level H bridge multilevel inverter. One switching element and four diodes added in the conventional full-bridge inverter are connected to the centre tap of dc power supply.

Proper switching control of the auxiliary switch can generate half level of dc supply voltage. It has five output voltage levels that are \( 0, V_s/2, V_s, -V_s/2, -V_s \).

![Fig. 1: A configuration of the single-phase five-level PWM inverter](image)

The switching combinations are shown in Table 1.

<table>
<thead>
<tr>
<th>ON switches</th>
<th>Node A voltage (V_a)</th>
<th>Node B Voltage (V_b)</th>
<th>Output Voltage (V_{AB}=V_a)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S_1, S_4</td>
<td>V_s</td>
<td>0</td>
<td>V_s</td>
</tr>
<tr>
<td>S_2, S_3</td>
<td>V_s/2</td>
<td>0</td>
<td>V_s/2</td>
</tr>
<tr>
<td>S_2, S_4</td>
<td>0 (V_s)</td>
<td>0 (V_s)</td>
<td>0</td>
</tr>
<tr>
<td>S_1, S_5</td>
<td>0</td>
<td>V_s/2</td>
<td>-V_s/2</td>
</tr>
<tr>
<td>S_2, S_5</td>
<td>0</td>
<td>V_s</td>
<td>-V_s</td>
</tr>
</tbody>
</table>
For the output voltage $V_s$, the switches $S_1, S_4$ need to be turned on.

![Fig. 2(a): State 1: $V_o = V_s$; $i_o = (+ve)$](image)

For the output voltage $V_s/2$, switches $S_4, S_5$ need to be turned on.

![Fig. 2(c): State 3: $V_o = V_s/2$; $i_o = (+ve)$](image)
Fig. 2(d): State 4: $V_o = V_s/2$ ; $i_o = (-ve)$

For the output voltage 0, either switches $S_3, S_4$ or $S_1, S_2$ need to be turned on.

Fig. 2(e): State 5: $V_o = 0$ ; $i_o = (+ve)$

Fig. 2(f): State 6: $V_o = 0$ ; $i_o = (-ve)$

For the output voltage $-V_s/2$, switches $S_3, S_5$ need to be turned on.
Fig. 2(g): State 7: \( V_o = \frac{-V_s}{2} \) ; \( i_o = (+ve) \)

Fig. 2(h): State 8: \( V_o = \frac{-V_s}{2} \) ; \( i_o = (-ve) \)

For the output voltage \(-V_s\), switches \(S_2, S_3\) need to be turned on.

Fig. 2(i): State 9: \( V_o = -V_s \) ; \( i_o = (+ve) \)
The operation of a TCHB inverter can be divided into ten switching states. Operational states of the conventional inverter are shown in Fig. 2(a), (b), (e), (f), (i), and (j) in sequence, and additional states in the proposed inverter synthesizing half level of dc bus voltage are shown in Fig. 2(c), (d), (g), and (h).

2.2 Modified Topology:
The main drawback of the above configuration is the inability to tolerate faults on the switches of two legs. In such situations, the operation is stopped until the faulted device gets changed. Hence, to overcome this drawback a few modifications were done. So, instead of two H-bridge legs, one leg of H-bridge (i.e., “Leg-I”) & one leg of an NPC (i.e., Leg-II) are used as shown in Fig. 3.

This modification is then powered using a single DC source along with two series connected electrolytic capacitors whose voltage remains in balance state with suitable switching topology regardless of modulation factor or load dynamics. This modified topology can generate a five-level output voltage (i.e., $V_S, V_S/2, 0, -V_S/2, -V_S$). The two capacitors in series will get charged into half of the DC supply voltage. To achieve a higher number of output levels cascading of the modified topology is proposed.

Working levels:
a. For output voltage $V_S$: Switches $S_1, S_5, S_6$ are switched ON. This level has no impact on the capacitor voltages & in both conditions ($i_L > 0$ and $i_L < 0$) the load current is generated by the DC source alone.
b. For output voltage of $V_S/2$: Switches $S_5, S_6, S_7$ are switched ON. At this level, two cases occur, i.e. ($i_L > 0$ and $i_L < 0$). Depending on the current direction the capacitor $C_2$ either charges ($i_L < 0$) or discharges ($i_L > 0$).
c. For output voltage of 0: Switches $S_4, S_5, S_7$ are switched ON. In both, the conditions ($i_L > 0$ and $i_L < 0$) the load current is generated by the DC source alone.
d. For output voltage of $-V_S/2$: Switches $S_3, S_4, S_7$ are switched ON. At this level, two cases occur, i.e. ($i_L > 0$ and $i_L < 0$). Depending on the current direction the capacitor $C_2$ either charges ($i_L > 0$) or discharges ($i_L < 0$).
e. For output voltage of $-V_S$: Switches $S_2, S_3, S_4$ are switched ON. This level has no impact on the capacitor voltages & in both conditions ($i_L > 0$ and $i_L < 0$) the load current is generated by the DC source alone.
Fault tolerant strategies:
As the modified topology is a combination of CHB leg and NPC leg, the faults are classified based on the switches of leg mentioned above, which are summarised in Table 3. The steps to be followed under fault condition are:

a) Isolate the leg connection of faulted switch with the help of fast fuses.
b) Modify the modulation index to half.
c) Update the switching strategy as per Table 3.

For this modified topology the fault-tolerant strategies are a fault on leg-I (i.e., Either both switches are open, or one of the switches is opened or one switch open while the other being short).

The switching states of the modified topology are shown in table 2.

<table>
<thead>
<tr>
<th>Output Voltage</th>
<th>ON state switches</th>
<th>Effect on capacitor if ( i_L &gt; 0 )</th>
<th>Effect on capacitor if ( i_L &lt; 0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_s )</td>
<td>( S_1, S_5, S_6 )</td>
<td>No effect</td>
<td>No effect</td>
</tr>
<tr>
<td>( V_s/2 )</td>
<td>( S_5, S_6, S_7 )</td>
<td>Capacitor discharges</td>
<td>Capacitor charges</td>
</tr>
<tr>
<td>0</td>
<td>( S_4, S_5, S_7 )</td>
<td>No effect</td>
<td>No effect</td>
</tr>
<tr>
<td>( -V_s/2 )</td>
<td>( S_3, S_4, S_7 )</td>
<td>Capacitor charges</td>
<td>Capacitor discharges</td>
</tr>
<tr>
<td>( -V_s )</td>
<td>( S_2, S_3, S_4 )</td>
<td>No effect</td>
<td>No effect</td>
</tr>
</tbody>
</table>

The current path for modified topology for each state along with the effect of a capacitor is shown in Fig.4.
Fig. 4(c): Output voltage = $V_s$

Fig. 4(d): Output voltage = $V_s$

Fig. 4(e): Output voltage = 0 V
Fig. 4(f): Output voltage = 0 V

Fig. 4(g): Output voltage = \(-\frac{V_s}{2}\) (capacitor charging)

Fig. 4(h): Output voltage = \(-\frac{V_s}{2}\) (capacitor discharging)
Analysis of modified topology under fault conditions on Leg-I:

1. Both $S_1$ or $S_2$ are Open:

The leg-I is composed of the CHB switch configuration hence consists of two main switches ($S_1$ & $S_2$). Under a fault state on $S_1$, the voltage of the capacitor $C_1$ decreases slightly, and the voltage of the capacitor $C_2$ increases slightly, this drop and rise in voltages are due to the prominence of the inductor on the load. Similarly, under a fault state on $S_2$, the voltage of capacitor $C_1$ increases and the voltage of capacitor $C_2$ decreases.

When the fault is cleared, and control strategy is reconfigured the respective capacitor voltage again come back to half of the DC source voltage due to the self-voltage balancing capability of the presented inverter.
Fig. 5(b) Output voltage = 0 V

Fig. 5(c) Output voltage = \(-V_s/2\) (capacitor charging)

Fig. 5(d) Output voltage = \(V_s/2\) (capacitor charging)
2. $S_1$ is open, and $S_2$ is Short:
Due to this fault on leg-I, we get a two-level output as one switch is shorted, the entire voltage comes across switch, and we get $-V_S$ and 0. The switching state modified topology under this fault condition is given in table 4. Current flow path in case of the fault is shown in fig 6.

Table 4: switching state modified topology under the fault condition

<table>
<thead>
<tr>
<th>Output Voltage</th>
<th>ON state switches</th>
<th>Effect on capacitor if $i_L &gt; 0$</th>
<th>Effect on capacitor if $i_L &lt; 0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$S_4, S_5, S_7$</td>
<td>No effect</td>
<td>No effect</td>
</tr>
<tr>
<td>$-V_S$</td>
<td>$S_2, S_3, S_4$</td>
<td>No effect</td>
<td>No effect</td>
</tr>
</tbody>
</table>
3. **$S_1$ is Short, and $S_2$ is Open:**

   Due to this fault on leg-I, we get a two-level output as switch $S_1$ is shorted, the entire voltage comes across switch, and we get $V_S$ and 0. The switching state modified topology under this fault condition is given in table 5. Current flow path in case of the fault is shown in fig 7.
Table 5: Switching state modified topology under the fault condition

<table>
<thead>
<tr>
<th>Output Voltage</th>
<th>ON state switches</th>
<th>Effect on capacitor if $i_L &gt; 0$</th>
<th>Effect on capacitor if $i_L &lt; 0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$S_4, S_5, S_7$</td>
<td>No effect</td>
<td>No effect</td>
</tr>
<tr>
<td>$V_S$</td>
<td>$S_1, S_5, S_6$</td>
<td>No effect</td>
<td>No effect</td>
</tr>
</tbody>
</table>

Fig. 7(a): Output voltage = 0 V

Fig. 7(b): Output voltage = 0 V

Fig. 7(c): Output voltage = $V_S$
III. CONTROL STRATEGY OF TCHB FIVE-LEVEL MULTILEVEL INVERTER:

3.1 CONVENTIONAL TOPOLOGY:

The topology used for generating the switching pulses Multi-Carrier Phase Shifted Pulse Width Modulation (MCPSPWM). In the multicarrier modulation technique, the amplitude and frequency of all triangular carriers are similar in addition to the phase shifts between adjacent carriers.

In this MCPWM scheme, the carrier signals are compared with the reference signal and the gating pulses so obtained are used for switching of the devices corresponding to their respective voltage levels [25]. Under normal operating conditions, the modulation index is near to unity, whereas under the faulty condition the modulation index is reduced to half. Fig. 8 shows the modulation strategy executed for obtaining the pulses for individual switches.

![Diagram](image)

Fig. 7(d): Output voltage = $V_s$

So, here in one cycle, the reference signal is divided into nine different modes:

- $a_0 = 0 < t < t_1$ and $t_4 < t < t_5$ and $t_7 < t < 0.02$
- $a_1 = t_1 < t < t_2$ and $t_3 < t < t_4$
- $a_2 = t_2 < t < t_3$
- $a_{-1} = t_5 < t < t_6$ and $t_7 < t < t_8$
- $a_{-2} = t_6 < t < t_7$

By using logical operators switching pulses for the switches can be obtained as:

- $S_1 = a_2$
- $S_2 = a_0 + a_{-2}$
- $S_3 = a_{-1} + a_{-2}$
- $S_4 = a_0 + a_1 + a_2$
- $S_5 = a_1 + a_{-1}$

By using the above combinational logic, the switching pulses are obtained.
3.2 MODIFIED TOPOLOGY:

The gating pulses for the switches in this topology is provided by using suitable Multi-Carrier Pulse Width Modulation (MCPWM) technique with a carrier frequency of 5kHz and reference signal frequency of 50Hz.

In this MCPWM scheme, the carrier signals are compared with the reference signal and the gating pulses so obtained are used for switching of the devices corresponding to their respective voltage levels [25]. Under normal operating conditions, the modulation index is near to unity, whereas under the faulty condition the modulation index is reduced to half. Fig.9 shows the modulation strategy executed for obtaining the pulses for individual switches.

So, here in one cycle, the reference signal is divided into nine different modes:

- \( a_0 = 0 < t < t_1 \) and \( t_4 < t < t_5 \) and \( t_8 < t < 0.02 \)
- \( a_1 = t_1 < t < t_2 \) and \( t_3 < t < t_4 \)
- \( a_2 = t_2 < t < t_3 \)
- \( a_{-1} = t_5 < t < t_6 \) and \( t_7 < t < t_8 \)
- \( a_{-2} = t_6 < t < t_7 \)

By using logical operators switching pulses for the switches can be obtained as:

- \( S_1 = a_2 \)
- \( S_2 = a_{-2} \)
- \( S_3 = a_{-1} + a_{-2} \)
- \( S_4 = a_0 + a_{-1} + a_{-2} \)
- \( S_5 = a_0 + a_1 + a_2 \)
- \( S_6 = a_1 + a_2 \)
- \( S_7 = a_0 + a_1 + a_{-1} \)

By using the above combinational logic, the switching pulses for normal operating conditions are obtained and showed in Fig. 10.

Under a fault condition on the switches of leg-I, only the modulation index is modified while the switching scheme remains the same as of in the normal state. It must be noted that, once the fault occurs, the faulty state persists for 160ms (i.e., for eight cycles), after that the switching strategy is modified according to Table 3.
IV. SIMULATION & RESULTS:

The conventional TCHB based five-level MLI using LS-POD PWM has been simulated, and the output voltage and current waveforms and THD have been observed.

Fig.11: Conventional five level TCHB multilevel inverter

Fig.12: Output Current and Voltage Waveform of conventional five level TCHB multilevel inverter

Fig.13: Conventional Five level TCHB multilevel inverter with multicarrier modulation, THD=39.34%.
The Modified TCHB based five-level MLI using LS-POD PWM has been simulated, and the output voltage and current waveforms and THD have been observed.

Fig. 14: Modified Five level TCHB multilevel inverter

Fig. 15: Output Voltage and Current Waveform of Modified Five level TCHB multilevel inverter
The Modified TCHB based five-level MLI using LS-POD PWM under fault conditions (Leg-I) has been simulated, and the output voltage and current waveforms and THD have been observed.

Fig.16: Modified Five level TCHB multilevel inverter, THD=4.44%

Fig.17: Modified Five level TCHB multilevel inverter under fault conditions (Leg-I opened)
Fig. 18: Output current and voltage waveforms for a Modified Five level TCHB multilevel inverter under fault conditions (Leg-I opened)

Fig. 19: Modified Five level TCHB multilevel inverter under post-fault conditions (Leg-I opened), THD=2.97%

The modified Five level TCHB multilevel inverter using level shifted phase opposition disposition PWM technique when under fault conditions (Leg-I, i.e., $S_1$ open & $S_2$ shorted) and the output voltage and current waveforms have been observed.
Fig. 20: Modified Five level TCHB multilevel inverter under fault conditions (Leg-I, i.e., $S_1$ open & $S_2$ shorted)

Fig. 21: Output current and voltage waveforms for Modified Five level TCHB multilevel under fault conditions (Leg-I, i.e., $S_1$ open & $S_2$ shorted)

The modified Five level TCHB multilevel inverter using level shifted phase opposition disposition PWM technique when under fault conditions (Leg-I, i.e., $S_2$ open & $S_1$ closed) has been simulated and the output voltage and current waveforms have been observed.
Fig. 22: Modified Five level TCHB multilevel inverter under fault conditions (Leg-I, i.e., $S_2$ open & $S_1$ closed)

Fig. 23: Output waveforms for Modified Five level TCHB multilevel inverter under fault conditions (Leg-I, i.e., $S_2$ open & $S_1$ closed)
V. RESULTS:

The comparative analysis for a conventional five-level TCHB topology and modified five-level TCHB topology is studied, and the results are shown in Table 6.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Conventional five-level TCHB topology</th>
<th>Modified five-level TCHB topology</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PD</td>
<td>POD</td>
</tr>
<tr>
<td>Switches of blocking voltage $V_s$</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Switches of blocking voltage $V_s$</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Total number of switches</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>DC source</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Capacitor</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Reliability in case if a fault on Leg-I</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Reliability in case if a fault on Leg-II</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Efficiency</td>
<td>91.2%</td>
<td>97.46%</td>
</tr>
</tbody>
</table>

Table 6: Comparison of TCHB five-level topologies

VI. CONCLUSION:

A five-level Transistor Clamped H-bridge based Cascaded Multilevel Inverter (TCHB) with multicarrier pulse width modulation is simulated. The simulation results prove that the Total Harmonic Distortion (THD) for a TCHB MLI is low using Multi-Carrier Modulation method when compared with a conventional cascaded multilevel inverter. This circuit also decreases the number of switches, sources, and losses. The total harmonic distortion for the presented model is observed.

The main demerit of conventional topology is the inability to tolerate faults on the switches of both its legs. Hence the conversion operation is halted until the faulted device gets replaced. To overcome this inability tolerating the fault in TCHB inverter, some alterations are done, i.e., instead of on two legs of H-bridge, one leg of H-bridge (termed as ‘leg-I’) and one leg of NPC (termed as leg-II) is used so that the reliability is improved.

This modified topology also has the additional merit of self-voltage balancing of its capacitor voltage even under post-fault conditions. The THD for the modified topology under normal and fault conditions have been observed and is improved by adding an LC filter to the modified topology whose value is less than that of a conventional TCHB five-level multilevel inverter.

The performance analysis of a TCHB based five-level multilevel inverter topologies has been studied, and the results have been tabulated.

REFERENCES:


