Grid Connected Multilevel Power Converter for Renewable Energy Systems

Murali Krishna Patnala, Kampa Narendra Babu
Department of EEE, Godavari Institute of Engineering & Technology (A), Rajahmundry, Andhra Pradesh, India.

Abstract : This paper emphasis on Grid connected multilevel topologies for single-phase converters, Multilevel topologies allow to reduce the harmonic content of the converter output voltage, allowing the use of smaller and cheaper output filters. Moreover, these topologies are usually characterized by a strong reduction of the switching voltages across the switches, allowing the reduction of switching losses and electromagnetic interference (EMI). The main objective of this paper is a novel five-level converter based on a full-bridge topology with diodes connected to the midpoint of the dc link to balance the midpoint voltage, an intelligent controller like a specific fuzzy logic PWM strategy to be developed to keep the output voltage being sinusoidal and to have the high efficient performance. This solution is opted for renewable energy systems, like where unity power factor operations are commonly required. This model circuit realized in MATLAB-SIMULINK software and Simulation results illustrate the effectiveness of the proposed solution.

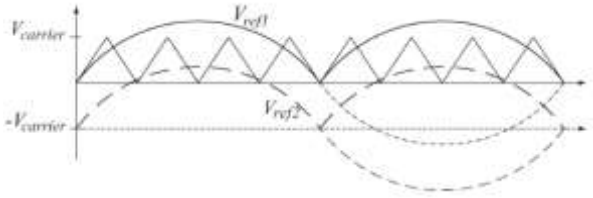
Keywords-**Multilevel inverter,Hybrid PWM,Fuzzy logic, Renewable systems.**

I. INTRODUCTION

The require for renewable energy has increased significantly over the years because of shortage of fossil fuels and greenhouse effect. PV inverter, which is the heart of a PV system. Enhance the output waveform of the inverter reduces its respective harmonic content and the size of the filter used and the level of electromagnetic interference (EMI) generated by operation of the inverter. In recent developments, multilevel inverters have become more attractive due to their advantages over conventional multilevel pulse width-modulated (PWM) inverters. They offer improved output waveforms, smaller filter size, lower total harmonic distortion (THD), lower EMI, and others [3]–[8].

A typical single-phase and three-level inverter adopts full-bridge configuration by using estimated sinusoidal modulation technique as the power circuits. The harmonic components of the output voltage are resolve by the carrier frequency and switching functions. Therefore, their harmonic reduction is restricted to a certain degree [4].

To overcome this limitation, this paper describes a five-level PWM inverter whose output voltage can be given in the following five levels are like: zero, $+1/2$Vdc, Vdc, $-1/2$Vdc, and $-$Vdc. As the number of output levels raised, the harmonic content can be condensed. This inverter topology uses two reference signals, as an alternative of one reference signal, to generate PWM signals for the switches. Both the reference signals V_{ref1} and V_{ref2} are indistinguishable to each other, apart from for an offset value equivalent to the amplitude of the carrier signal $V_{carrier}$.



Carrier and reference signals

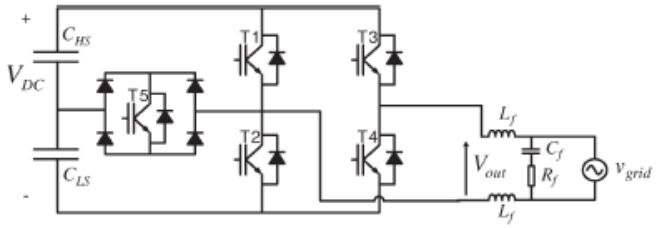
Because the inverter is used in a PV system, a proportional–integral (PI) current control scheme is in use to keep the output current sinusoidal and to have high dynamic performance under rapidly changing atmospheric conditions and to keep the power factor at near unity.

This paper is organized as follows. Section II follows the five-level inverter topology and PWM law. In Section III, the proposed inverter topology and the operational principle. Section IV gives the midpoint voltage control (MVC) for the the two capacitors of the dc link. Section V briefly deals with the designing the fuzzy controller in application of the proposed solution to renewable energy systems. Section VI presents a very brief analysis simulation results. Section VII presents the conclusions.

II. FIVE LEVEL INVERTER TOPOLOGY AND PWM LAW

The single-phase five-level inverter topology proposed circuit diagram is shown in Fig. 2. The converter is constituted by a full bridge with an supplementary bidirectional switch (realized with an IGBT and four diodes), employed to connect the midpoint of the dc link to the converter output. The energy

efficiency of this solution is potentially very high; however, the capacitor's voltage balancing is not taken into account.

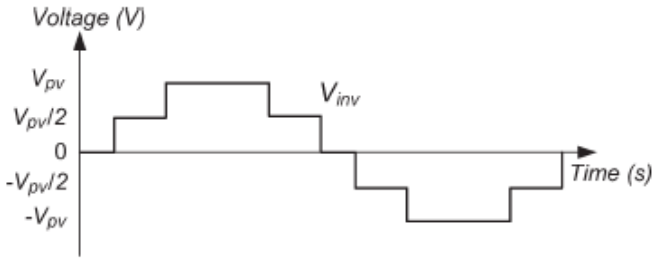


Proposed Five-level Full Bridge topology

The proposed inverter is used in a grid-connected PV system utility grid is used as an alternative of load. The dc–dc boost converter is used to step up inverter output voltage V_{inv} to be more than $\sqrt{2}$ of grid voltage V_g to ensure power flow from the PV arrays into the grid. A filtering inductance L_f is used to filter the current introduce into the grid. The injected current must be sinusoidal with low har monic distortion. In order to generate current in sinusoidal form, sinusoidal PWM is used because it is one of the most effective methods. Sinusoidal PWM is to attain by comparing a high-frequency carrier with a low-frequency sinusoid, which is the modulating or reference signal. The carrier signal has a constant period; therefore, the switches have constant switching frequency. The switching instant is resolve from the crossing of the carrier and the modulating signal.

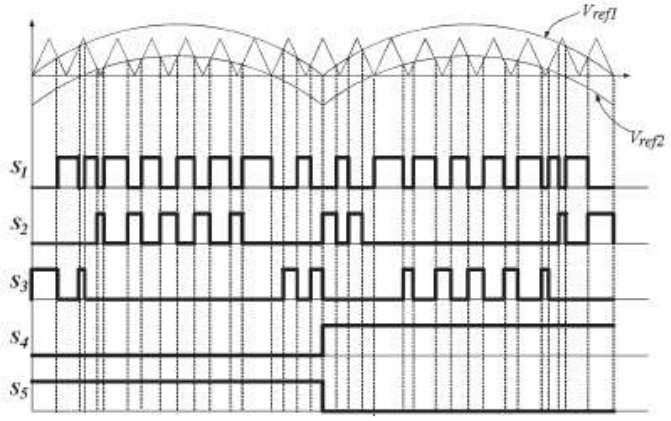
III. Operational Principle Of The Proposed Inverter

PV arrays are input voltage sources, the voltage produced by the arrays is known as V_{arrays}. V_{arrays} is boosted by a dc–dc boost converter to exceed $\sqrt{2}$ V_g. The voltage across the dc-bus capacitors is known as V_{pv}. The working principle of the proposed inverter is to generate fivelevel output voltage, like given as zero, $+V_{pv}/2$, $+V_{pv}$, $-V_{pv}/2$, $-V_{pv}$ as in Fig. 3. As shown in Fig. 2, an supplementary circuit which consists of four diodes and a switch S_1 is placed among the dc-bus capacitors and the full-bridge inverter. Proper switching control of the auxiliary circuit can generate semi level of PV supply voltage, i.e., $+V_{pv}/2$ and $-V_{pv}/2$ [4].



Ideal Five Level Inverter out put voltage V_{inv}

Two reference signals V_{ref1} and V_{ref2} will take turns to be differentiate with the carrier signal at a time. If V_{ref1} exceeds the peak amplitude of the carrier signal $V_{carrier}$, V_{ref2} will be evaluating with the carrier signal until it reaches zero.



Switching pattern for Single phase five level inverter.

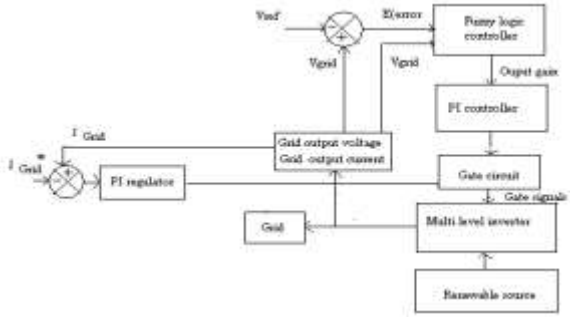
At this point onward, V_{ref1} takes over the evaluation process until it exceeds $V_{carrier}$. It can lead to a switching pattern, as shown in Fig. 4. Switches S_1–S_3 switches at the rate of the carrier signal frequency, whereas S_4 and S_5 will operate at a frequency corresponding to the fundamental frequency. Table I shows the level of V_{inv} during S_1–S_5 switch on and off.

TABLE 1 : INVERTER OUTPUT VOLTAGE DURING S_1 –S_5 SWITCH ON AND OFF

S1	*S2*	*S3*	*S4*	*S5*	V_{inv}
ON	*OFF*	*OFF*	*OFF*	*ON*	*+Vpv/2*
OFF	*ON*	*OFF*	*OFF*	*ON*	*+Vpv*
OFF	*OFF or (ON)*	*OFF or (ON)*	*(ON) or (OFF)*	*ON or (OFF)*	*0*
ON	*OFF*	*OFF*	*ON*	*OFF*	*-Vpv/2*
OFF	*OFF*	*ON*	*ON*	*OFF*	*-Vpv*

IV. CONTROL SYSTEM ALGORITHM AND IMPLEMENTATION

The control system Block diagram of the proposed Multilevel inverter is shown in the Fig 5.



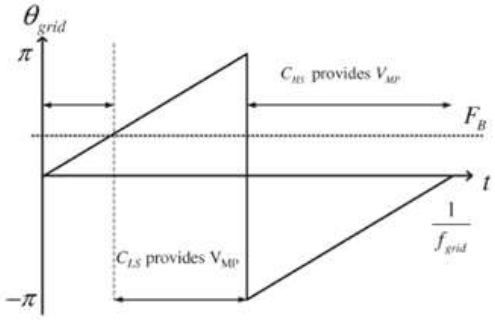
Block diagram of proposed Multilrvrl inverter with control system

The feedback controller utilizes the PI algorithm. As shown in Fig. 5, the current inject into the grid, also known as grid

current I_g, is sense and feed back to a comparator which compares it with the reference current I_{ref}. I_{ref} is attaining by sensing the grid voltage and converting it to reference current and multiplying it with constant m. This is to make certain that I_g is in phase with grid voltage V_g and always at near-unity power factor. One of the problems in the PV systems is the amount of the electric power generated by solar arrays always changing with weather conditions, the intensity of the solar radiation. A maximum power point tracking (MPPT) method or algorithm, which has fast response characteristics and is able to make good use of the electric power generated in any weather, is needed to solve the aforementioned problem. Various MPPT control methods have been discussed in detail in [2]. Constant m is derived from the MPPT algorithm.

The block scheme of the Midpoint Voltage Control (MVC) [1]-[2]. The capacitors swap for the midpoint voltage regulation relies on the corresponding factor F_B, which is provided by a proportional integral (PI) regulator. The input of the PI regulator is the difference between the moving averages ($T_{average} = T_{grid\_voltage}$) of V_{MP} and $V_{dc}/2$. The dotted part in Fig. 5 shows a simple closed-loop control (PI + feedforward) of the injected grid current i_{grid} used for simulation results. In order to fix V_{MP}, the five-level modulator works in this way: the corresponding factor F_B is compared with θ_{grid} (see Fig. 6), and the V_{MP} voltage is provided to the full-bridge rails from the capacitor C_{LS} or C_{HS} through the simple law shown in

$$\begin{cases} \theta_{grid} \geq F_B \rightarrow C_{LS}, & provides \quad V_{MP} \\ \theta_{grid} < F_B \rightarrow C_{HS}, & provides \quad V_{MP} \end{cases} \qquad (1)$$



MVC working in case of a positive F_B.

In symmetric conditions, $F_B = 0$, the V_{MP} voltage is gives by the low-side capacitor C_{LS} during the whole positive semi period and by the high-side capacitor C_{HS} during the whole negative semi period. If an asymmetry arises and, for example, V_{MP} tends toward a lower

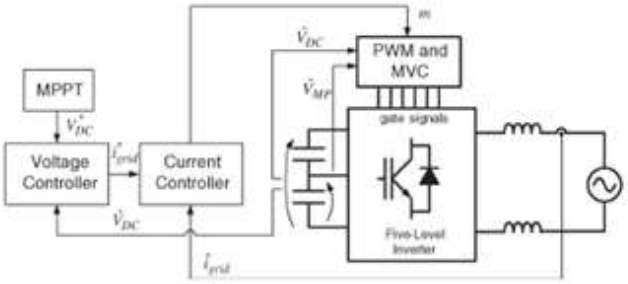
value, the MVC will use for a lengthy time interval C_{HS} to provide V_{MP} to the full-bridge rails. In this case the MVC will impose a positive F_B. Fig. 6 presents this situation: the time in which the additional voltage V_{MP} is provided by C_{LS} is less than half of the period. During the remaining time, V_{MP} is provided by C_{HS}. It is to be noted that the MVC does not increase the number of commutations in a PWM period. The balancing factor F_B affects the expression (5) by changing the sign of I_{MP} at a grid voltage angle different from zero. The expression of I_{MP} that considers the balancing factor can be rewritten as

$$I_{MP}(\theta_{grid}, F_B) = \begin{cases} |i_{grid}| & D(m)\,\mathrm{sgn}(\theta_{grid} - F_B), |m| > 0.5 \\ |i_{grid}| & (1 - D(m))\,\mathrm{sgn}((\theta_{grid} - F_B), |m| > 0.5 \end{cases} \quad (2)$$

This means that the average value of I_{MP} over a grid voltage period will be different from zero, and V_{MP} will vary according to (2). The variation of the midpoint voltage over a grid period can be evaluated by integrating (2) over a grid voltage period

$$\Delta V_{MP}(F_B) = -\frac{T_{grid}}{4\pi C}\int I_{MP}(\theta_{grid}, F_B)\, d\theta_{grid} \quad (3)$$

In Fig. 7, $\Delta V_{MP}(F_B)$ was evaluated over the interval $F_B \in [0, \pi/2]$ for a capacitance value $C = 2mF$ at different value of A and I_{grid}. If the value of A is small, i.e., V_{dc} is much greater than V_{grid}, In a similar way, $\Delta V_{MP}(F_B$ will be greater at higher values of I_{grid}. From a control system point of view, the maximum gain of the transfer function between ΔV_{MP} and F_B will be at the maximum value of I_{grid} and at the minimum value of A. In order to tune the discrete-time PI regulator in Fig. 5, the parameters must be chosen in order to render the system stable in this worst case scenario, using standard control theory techniques. In any case, an asymmetry in the system is usually steady state or slow varying; therefore, the bandwidth of the balancing control is not an issue.



Block scheme of the proposed converter control in a renewable energy apllication

The perturb-and-observe algorithm is used to take out maximum power from PV arrays and deliver it to the inverter. The signal of instantaneous current error is fed to a PI controller. The integral term in the PI controller improves the tracking by dropping the instantaneous error between the reference and the actual current. The resulting error signal u gives from V_{ref1} and V_{ref2} and it is compared with a triangular carrier signal, and intersections are sought to produce PWM signals for the inverter switches.

The control system of the proposed topology with MVC fed by a renewable energy source is presented in Fig. 7, which concerns a single-stage structure. The dc source can be renewable sources.

The inner loop regulates the current injected into the grid, while the outer voltage loop fixes the dc-link voltage. In a single-stage solution, the dc link is directly connected to the energy source, and the logic onboard the converter regulates the dc-link voltage in order to extract the limit available power with an maximum power point tracking (MPPT) algorithm. In order to track the maximum power point during rapid variations of weather conditions, the injected grid current and the dc-link voltage will be subject to abrupt changes. In a double-stage converter, the proposed topology is preceded by a dc–dc converter, which implements the MPPT control, whereas the dc–ac converter works with a fixed dc-link voltage. In this configuration, the dc–ac converter will be focus on injected grid current variations.

Mathematical Formulation

The PI algorithm can be expressed in the continuous time domain as

$$u(t) = K_p e(t) + K_i \int_{\tau=0}^{\tau} e(\tau)\, d\tau$$

where

$u(t)$ control signal;

$e(t)$ error signal;

t continuous-time-domain time variable;

τ calculus variable of integration;

K_p proportional-mode control gain;

K_i integral-mode control gain.

$$P\,term: \quad K_p e(t) = K_p e(k)$$

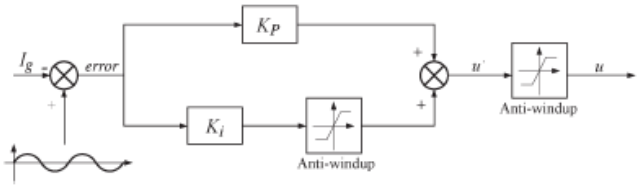
$$I\,term: \quad Ki\int e(\tau)d\tau \cong Ki\sum_{i=0}^{k}\frac{h}{2}[e(i)+e(i-1)]$$

Time relationship: $t = k * h$

where

h sampling period;

k discrete-time index: $k = 0, 1, 2, \ldots$



PI control algorithm

To eliminate the require to calculate the full summing up at each time step (which would require an ever-increasing amount of computation as time goes on), the summary is expressed as a running sum from which one can construct the discrete-time PI control law as

$$sum(k) = sum(k-1) + [e(k) + e(k-1)]$$

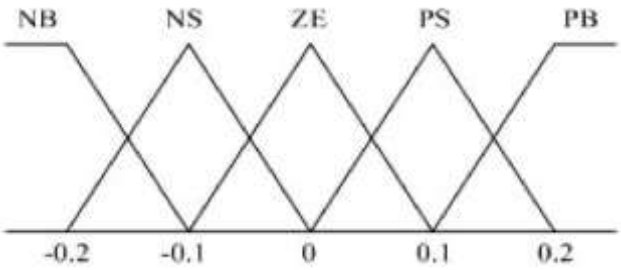
$$u(k) = K_p e(k) = K_i' sum(k).$$

These two equations, which represent the discrete-time PI control law, are implemented and is to control the overall operation of the inverter.

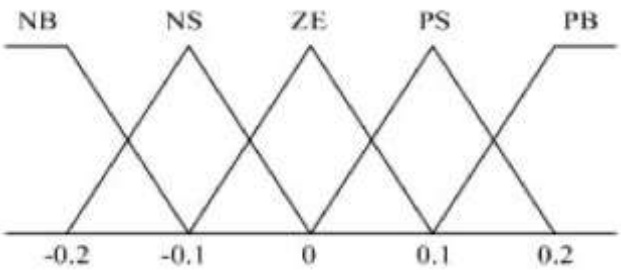
V. Design of Fuzzy Logic Controller

The design of a fuzzy controller requires the choice of variables (parameters) and the definition of membership functions. In this paper the membership functions chosen for parameter $E(error)$ are shown in Fig. 9, those chosen for parameter ΔE(Change in Error) are shown in Fig. 10, where the labels "NB" is negative-big, "NS" is negative-small, "ZE" is zero, and so forth. The fuzzy inference rules are summarized in Table II. The logic of the inference rules is:

- while $E_{(error)}$ is equal to ZE, the current state is correct that means that the inverter preserves the current state
- considering a generic state, if ΔE is positive ($V_{output\ inverter} > V_{ref}$) it is necessary to reduce the inverter state
- on the other hand, if ΔE is negative ($V_{output\ inverter} < V_{ref}$) it is necessary to increase the inverter state. A shifting mechanism has been



Membership functions of parameter E



Membership functions of parameters ΔE(Change in Error) and output.

implemented for balancing power distribution among the circuit of the H-bridge. The defuzzification process is done through the centre of gravity method.

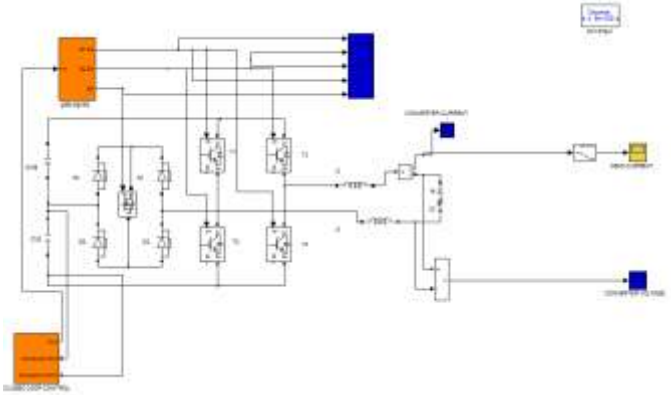
TABLE 2: FUZZY INFERENCE RULES

ΔE / E	NB	NS	ZE	PS	PB
NB	NB	NB	NB	NS	ZE
NS	NB	NB	NS	ZE	PS
ZE	NB	NS	ZE	PS	PB
PS	NS	ZE	PS	PB	PB
PB	ZE	PS	PB	PB	PB

If the error(E) Negative Big (NB) and change in error is NB the output of the controller is NB and so on. These rules formed as Table .II.

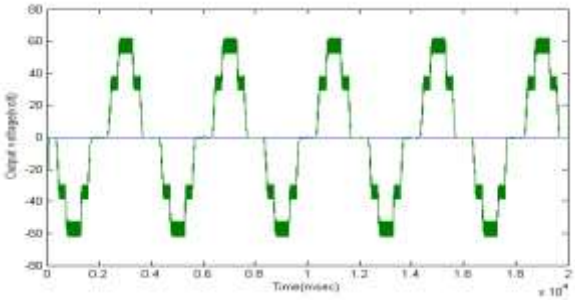
VI. SIMULATION RESULTS

The proposed five-level solution was simulated using the PLECS toolbox, which allows fast simulation of power electronic circuits under the MATLAB-SIMULINK environment. In Fig. 3,

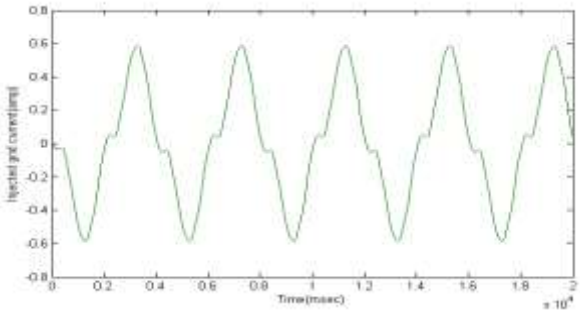


Simulation diagram for Proposed system

the simulation parameters were V_{dc} = 400 V, V_{grid} = 230 √ $2sin(2\pi 50t)$, C_{HS} = C_{LS} = $2mF$, L_f = 1000 μH, C_f = 2 μF, and R_f = 0.5Ω. A grid impedance Z_{grid} = $(j\omega 50\mu H + 0.4)\Omega$ was considered. The switching frequency was 20 kHz. The power converter control, formed by the MVC and the current controller, was the same with that shown in the block scheme

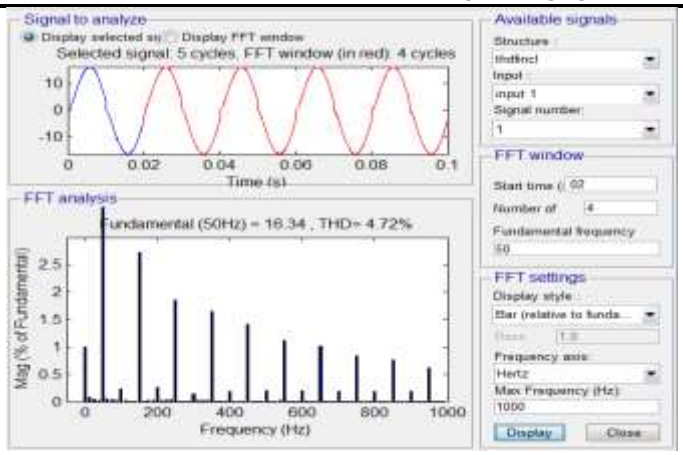


Converter ouput voltage



Grid injected current

The FFT of the output voltage (V_{out}) waveforms of the proposed solution and of the full-bridge topology driven by Hybrid PWM are shown in Fig. 14, %THD of injected grid current is 4.72%.



%THD of Injected grid current

VII. CONCLUSION

This paper gives conclusion on a novel five-level solution for single-phase grid-connected converters. The PWM strategy was chosen in order to get the minimum number of commutations to maximize efficiency. The PWM strategy developed; furthermore, an effective balancing control (i.e., MVC) was realized. It is important to note that the fivelevel output voltage is assured only with unity power factor operations. Simulations results showed the feasibility of the proposed converter architecture and the capability of the MVC to compensate for system asymmetries.

REFERENCES

[1] Giampaolo Buticchi, , Emilio Lorenzani, Giovanni Franceschini, "A Five-Level Single-Phase Grid-Connected Converter for Renewable Distributed Systems IEEE transactions on Industrial Eelectronics, vol. 60, no. 3,Pp.906-918, march 2013.

[2] T. Esram and P. L. Chapman, "Comparison of photovoltaic array maximum power point tracking techniques," *IEEE Trans. Energy Convers.*, vol. 22, no. 2, pp. 439–449, Jun. 2007.

[3] N. Rahim and J. Selvaraj, "Multistring five-level inverter with novel PWM control scheme for PV application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2111–2123, Jun. 2010.

[4] L. Zhang and S. Watkins, "Capacitor voltage balancing in multilevel flying capacitor inverters by rule-based switching pattern selection," *Elect. Power Appl.*, vol. 1, no. 3, pp. 339–347, May 2007.

[5] Y. Liang and C. Nwankpa, "A new type of statcom based on cascading voltage-source inverters with phase-shifted unipolar SPWM," *IEEE Trans. Ind. Appl.*, vol. 35, no. 5, pp. 1118–1123, Sep. 1999

[6] J. Leon, R. Portillo, S. Vazquez, J. Padilla, L. Franquelo, and J. Carrasco, "Simple unified approach to develop a time-domain modulation strategy for single-phase multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 9, pp. 3239–3248, Sep. 2008.

[7] J. Leon, S. Vazquez, A.Watson, L. Franquelo, P.Wheeler, and J. Carrasco, "Feed-forward space vector modulation for single-phase multilevel cascaded converters with any DC voltage ratio," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 315–325, Feb. 2009.

[8] Z. Cheng and B. Wu, "A novel switching sequence design for five-level NPC/H-bridge inverters with improved output voltage spectrum and minimized device switching frequency," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2138–2145, Nov. 2007.

[9] Y. Zhang and L. Sun, "An efficient control strategy for a five-level inverter comprising flying-capacitor asymmetric H-bridge," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4000–4009, Sep. 2011.

[10] D. Ruiz-Caballero, R. Ramos-Astudillo, S. Mussa, and M. Heldwein, "Symmetrical hybrid multilevel dc–ac converters with reduced number of insulated DC supplies," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 307–2314, Jul. 2010.