A REVIEW: PERFORMANCE ANALYSIS OF VOLTAGE CONTROLLED DIFFERENTIAL RING OSCILLATORS BASED ON DELAY CELL USING CMOS NANOTECHNOLOGY

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Abstract: Voltage controlled ring oscillators using differential topology have been designed and implemented for different applications using CMOS nanotechnology with the various characteristics. But all have different behaviors like some advantages and disadvantages and relate to each other. This paper presents a performance analysis of voltage controlled ring oscillators (VCRO) based on various differential delay systems in term of wide tuning range and low power consumption at below 1V input supply. This comparative analysis shows the simulative result of four types of VCROs. One of them has very low power consumption i.e. minimum 0.34µW for low power applications and other has maximum tuning range 1GHz-11.53GHz for broadband applications using CMOS nanotechnology as compare to others.

Keywords- Ring oscillator, Differential delay system, Wide tuning range, Low power consumption.

I. INTRODUCTION

From the previous decade of year, the voltage controlled oscillators are very popular building blocks in modern electronics industries for broadband communication applications and biomedical applications. The VCOs are mainly construct to design different systems such as Clock Recovery Systems, Phase Locked Loop Systems, and Frequency Synthesizers systems etc. [1][2][3]. The voltage controlled oscillator needs double operating frequency to achieve 50% duty cycle at high speed. Which makes difficult the designing of low power phase locked loop systems [4]. Therefore it is very challenging and difficult task to design ultra low power consumption with high tuning range voltage controlled ring oscillators for low power broadband applications.

In the present time, VCOs are designed and implemented with the help of different topology like - Differential topology, Current starved topology, Single ended topology, RC and LC network topology, Body bias and Replica bias topology etc. for specific applications. This paper shows the comparative analysis of designed five VCROs on the basis of differential topology with various number of delay stages. The simulated result measured in term of wide tuning range and low power consumption. The advantages of five different VCRO are discussed in section 2. All required structures with simulated results are compared and evaluate in section 3 with the conclusion in section 4.

II. DELAY CELLS FOR VOLTAGE CONTROLLED DIFFERENTIAL RING OSCILLATOR

Voltage controlled ring oscillator is having a delay cell connected by single ended topology and differential topology. In the single ended ring topology shown in fig-1, in which the odd number of delay cell is connected in the feedback form like the output of last stage is the input of first stage. The ideal condition for the sustained oscillations should be fulfill means 360° total phase shift around the loop and unity loop gain stated by the Barkhausen principle.

fig-1 single ended ring topology for vcro

According to the differential ring topology shown in fig-2, provide different phases (0°, 45°, 90°, 135°, 180°…). The phase difference between input and output voltage is required 225° for oscillation condition [5].
Hence, oscillations frequency for N stages is:

\[ f_0 = \frac{1}{2Nt_d} \]

Where, \( N \) = total number of delay cell  
\( t_d \) = delay time of each delay cell

The differential ring topology for VCO is useful to reject the common mode noise and avoid bypass coupling capacitors good stability and high frequency. Differential ring oscillator is composed of a load, which have active and passive elements both. It is on demand for wide tuning range, constant voltage swing, and low power consumption with very low noise. The differential delay system shown in fig-3 is used to design voltage controlled ring oscillator with three stage delay cell.

This delay system is designed with two PMOS transistors operate from deep triode region to saturation region and varied with Vgs of transistor. While two NMOS transistor is operated in only saturation region. The designed voltage controlled ring oscillator using this differential delay cell is very necessary to increase tuning range and reduce power consumption. By using this delay system, 3 stage VCRO has been designed for the wide tuning range 0.80GHz-11.64GHz with low power consumption 68.60µW at 1.2V input supply and 4.32 µW at 0.8V in 2014 [6]. While Saikee Chauhan has designed the 5 stage, 7 stage, 9 stage differentials VCRO by using simple CMOS delay cell shown in fig-4.

CMOS delay cell is consist of complementary MOS transistors. Where PMOS is used as a load and NMOS is used as driver for high current gain. These PMOS and NMOS have similar like channel length, doping. This delay cell is use as a Inverter means Vin = 0 then Vo =1 and vice-versa [7]. The differential VCRO using simple delay cell provides high frequency range up to MHz with power consumption in µW (min 0.34 µW). But this tuning range is low as compare to other for wide application. In year 2016, B. S. Patro
designed the low phase noise, wide tuning range differential VCRO for signal processing. He has designed proposed delay cell for specially high signal processing system shown in fig-5.

![fig-5 delay cell for 2 stage differential vcro](image)

The differential pair of P2 and P3 is use in positive feedback format to reduce the delay and increase the speed in oscillation of oscillator. The oscillator frequency can controlled by the Vc given in P0 and P1. The negative feedback circuit instead of positive feedback can induce more stability with high speed but consume more power. Hence this configuration of delay cell with positive feedback is useful to avoid the use of current mirror. The differential VCRO using this delay cell has provide the wide tuning range of 2.5GHz-7.7GHz and low power consumption 2.18 µW with very low phase noise of -96.47dBc/Hz [8].

Recently in 2019, Esteban Tlelo - Cuautle has designed the wide band VCRO with current-mode logic gate based on differential topology. It is implemented on CMOS nanotechnology. The current mode logic gate as a delay cell is shown in fig-6.

![fig-6 common mode logic gate as a delay cell for differential vcro](image)

The oscillation frequency of this VCRO is inversely depended on the number of common mode logic gate N and the propagation delay time t\textsubscript{d}. The delay can be reduced by transconductance of transistor with low equivalent capacitance. This VCRO provides the frequency ranges of 2.65–5.65 GHz with low power consumption [9].

### III. RESULTS OF SIMULATION

The four types of differential voltage controlled ring oscillator have designed using different delay cell for wide band applications and simulated on different technology. The VCRO using delay cell shown in fig-3 is simulated in LT spice tool. Fig-7(a) shows the transient response of VCRO at VDD = 1V and Vc =0.5V with Vgs = 2.5 V, while fig-7(b) shows the power dissipation varies with different power supply. The maximum power dissipation is 68.66 µW at 1.2 V input supply and minimum dissipation is 4.40 µW at 0.8 V input supply with 0.5V control voltage.
While differential VCRO using simple CMOS delay cell shown in fig-4 is simulated on cadence virtuso tool. For a voltage controlled ring oscillator, propagation delay is an important factor. Hence the transient analysis for 5-stage, 7-stage and 9 stage differential ring oscillator for the period of 0ns to 20ns is shown in fig-8(a), fig-8(b) and fig-8(c) respectively.

The power consumption analysis by the Bar graph is shown in fig-8(d) which shows the minimum consumption of power (0.34μW) for the 5-stage differential VCRO using Simple CMOS delay cell. When we increase the stages of delay cell then power consumption will increase simultaneously. The transient analysis of 2-stage differential VCRO using delay cell (fig-6) shows the frequency of operation at 5.176 GHz at 1V input supply in fig-9(a) with static power consumption 2.188 uW in fig-9(b). Similarly, it provide calculated
phase noise -96.148 dBc/Hz at 1 MHz offset. It is very low when tuned properly.

The differential VCRO using Common mode gates (shown in fig-6) is provide the oscillations between 2.65 GHz and 5.65 GHz by varying control voltage 0.2 V -0.9 V, which is a wide tuning range with 39mW power consumption. The transient analysis of this differential VCRO is shown in fig-10.

<table>
<thead>
<tr>
<th>Ref. and Year</th>
<th>Process Technology</th>
<th>Stage</th>
<th>Tuning Range</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>[6] 2014</td>
<td>50nm CMOS Technology</td>
<td>3</td>
<td>0.80GHz-11.64GHz</td>
<td>4.32µW at 0.8V</td>
</tr>
<tr>
<td>[7] 2016</td>
<td>45nm CMOS Technology</td>
<td>5</td>
<td>1032MHz</td>
<td>0.34 µW,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7</td>
<td>831MHz</td>
<td>0.48 µW,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>9</td>
<td>751MHz</td>
<td>0.61 µW</td>
</tr>
<tr>
<td>[8] 2016</td>
<td>45nm CMOS Technology</td>
<td>2</td>
<td>2.5 GHz-7.7 GHz</td>
<td>2.18µW</td>
</tr>
<tr>
<td>[9] 2019</td>
<td>180nm CMOS Technology</td>
<td>4</td>
<td>2.65 GHz-5.65 GHz</td>
<td>39mW</td>
</tr>
</tbody>
</table>

IV. CONCLUSION

Various types of differential VCROs have been designed by the authors based on various delay system. But mostly used differential VCRO are discussed in this paper. From which, differential delay system used in [6] and [7] are very capable and reliable for the wide tuning range (maximum 11.64GHz) and low power consumption (minimum 0.34µW) respectively in broadband signal processing applications as compare to others VCOs till now.
REFERENCES


Biography

Shiksha Jain was born in Aligarh (UP), India in 1984. She received the B.Tech degree Electronics & Communication Engineering from ACET, under UP Technical University, India in 2005, M.Tech. degree in Digital Electronics from Gautam Budh Technical University, India in 2011, pursuing Ph.D in Electronics from Dr. Rammanohar Lohia Awadh University, India from 2016. Currently she is an assistant professor in Electronics & Communication Engineering Department of Institute of Engineering and Technology under Dr. Rammanohar Lohia Awadh University, India. His research interest includes microprocessor, VLSI Design, Digital system and Electronics Circuit.