IJRAR.ORG E-ISSN: 2348-1269, P-ISSN: 2349-5138

INTERNATIONAL JOURNAL OF RESEARCH AND ANALYTICAL REVIEWS (IJRAR) | IJRAR.ORG

An International Open Access, Peer-reviewed, Refereed Journal

MODIFIED FULL SWING FULL ADDER BASED ON COMPLEMENTARY PASS TRANSISTOR LOGIC (CPL) FOR LOW POWER APPLICATIONS

T.Jyothi Rajasri[1], U.Prakash[1] , Y.Subhash[1], V.Sairam[1] , ,P. Arudra[2], Ch. Sridevi[3]

[1]UG scholar,Department of ECE, Bonam Venkata Challamaya Engineering College[A],Odalarevu-533210.

[2]Assistant Professor,Department of ECE, Bonam Venkata Challamaya Engineering College[A],Odalarevu-533210.

[3]Associate Professor,Department of ECE, Bonam Venkata Challamaya Engineering College[A],Odalarevu-533210.

Abstract

Low power consumption and high speed operation are major challenges in modern VLSI design. Full adders are fundamental building blocks in arithmetic circuits such as ALUs and DSP processors. This paper presents a modified full swing restored Complementary Pass Transistor Logic (CPL) based full adder designed for low power applications. The circuit is implemented and analyzed using Tanner EDA tools. Simulation results show that the CPL design significantly reduces power consumption and transistor count compared to conventional CMOS designs.

Keywords—Full Adder, CPL, CMOS, Low Power VLSI, Pass Transistor Logic

I. INTRODUCTION

In recent years, the rapid advancement in semiconductor technology has significantly increased the integration density and complexity of integrated circuits. Power consumption, delay, and area have become the primary design constraints in modern Very Large Scale Integration (VLSI) systems. With continuous scaling of CMOS technology, the number of transistors integrated on a chip increases rapidly, which results in higher power dissipation.

Low power design has become essential for battery-operated devices such as laptops, mobile phones, and portable electronic systems. The major sources of power dissipation in CMOS circuits include dynamic power due to switching activity, short circuit power, and leakage power.

Dynamic power dissipation can be expressed as:

$P = \alpha C_L V_{dd}^2 f$

where

α – switching activity factor

CL – load capacitance

Vdd – supply voltage

f – operating frequency

Among different digital circuits, adders play a crucial role in arithmetic operations. The efficiency of a digital system is greatly influenced by the performance of its full adder circuits. Therefore, designing low power and high speed full adders has become an important research area.

II. LITERATURE SURVEY

Full adders are widely used in arithmetic circuits such as multipliers, digital signal processors, and ALUs. Many full adder designs have been proposed in literature to improve speed and reduce power consumption.

a) Traditional 28T Static CMOS circuit

The traditional CMOS full adder consists of 28 transistors and is built on conventional static CMOS structure [13]. The design comprises 14 PMOS pull-up and 14 NMOS pull-down transistors. The main advantage of this design is the ability to produce full swing voltages. The drawbacks of this circuit are that it produces unwanted delays because sum realizes on Carry out signal, it dissipates more power and since the number of transistors is high, it occupies larger area. [2]. The structure of CMOS full adder.

b) Transmission Gates Full Adder

A full adder could be designed by using MUX and XOR. But this is illogical in a complementary CMOS (C²MOS) implementation. It turns in to great when MUX and XORs are executed as transmission gates [6]. Here over all 20T is used to design this Full Adder So power dissipation is high but less than 20T conventional CMOS Full adder circuit. The Transmission Gates logic (TG) Full Adder is as in figure3

c) CPL Full adder

Complementary Pass transistor logic (CPL) based Full Adder circuit comprises of complimentary inputs or outputs, not only NMOS pass transistor circuit but also output CMOS inverters. In addition to this, PMOS keeper circuit is used to reduce swing restoration and also for reduce static power consumption. This system comprises of two stage pass transistor network. In the first stage, the network is designed by applying true inputs to pass transistor logic and second stage is designed by applying complementary inputs to pass transistor logic [3]. The preeminent drawback of Full adder circuit using CPL is that in the NMOS network swing degradation has to be restored.

d) GDI based full adder

GDI technique is a high speed low power design technique and very extensible for digital combinatorial circuits designs. The GDI technique is power efficient because the number of transistors is minimum. So that delay and power consumption is minimum. The GDI cell includes three inputs: G (common gate input of PMOS and NMOS), P (input to the source or drain of PMOS), and N (input to the drain or source of NMOS). The PMOS and NMOS both the bodies are connected to P or N respectively. The main asset of GDI technique is that a wide range of logic functions can be designed by using single GDI cell. Only 5 PMOS and 5 NMOS transistors are used here. In total only 10 transistors are used to design the full adder. a,b,cin are the input and Carry out and sum are the output produced. Compared to other design techniques the number of transistor, delay and power dissipation is very much less. But the limitation of GDI technique is full swing restoration. This is because of threshold loss and to overcome this we have to use silicon on insulator or twin-well process to realize, which is very expensive. Another drawback is additional circuitry needed to give input to GDI circuits

e) 8T Modified GDI Full adder

The Modified GDI (MOD_GDI) technique is take up from the basic GDI technique to improve circuit performance. This new technique is benefit to minimize transistor number, reduce propagation delay and expenditure of total power. This design has three input terminals such as P, N and G and both the substrates of the NMOS and PMOS are connected to the GND and VDD. Figure 6 shows basic structure of Modified

GDI cell. 8T MGDI full adder has been implemented by using 3-input XOR for sum expression and 2-to-1 MUX have been used used for Carry out expression. [8]. It has low power consumption, delay and low power delay product as compared with GDI, CPL, CMOS techniques. By reducing count of transistors used has resulted in a great shrinkage in area and switching activity. Also there is noticeable contraction in power by reducing static and dynamic power dissipation that overall helps to improve the quickness of the design leading to the finest PDP

The larger part of the complex circuits could be reviving with less number of transistors, safekeeping the functionality and the constant output swing by using this modified GDI technique.

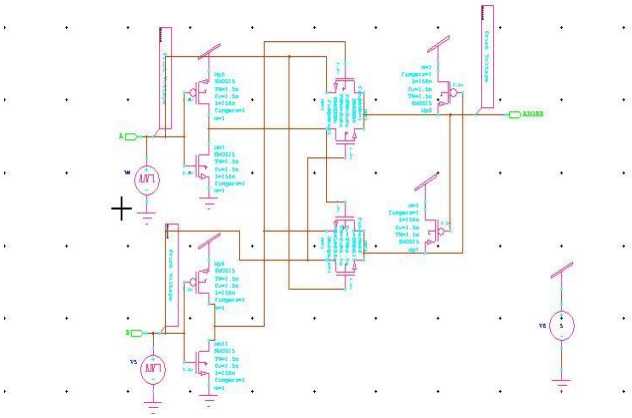


Fig. 1. CPL XOR transistor level diagram.

III. CPL

Complementary Pass Transistor Logic (CPL) is a digital circuit design technique that utilizes pass transistors in a complementary manner to implement logic functions efficiently. In CPL, logic gates are constructed using transmission gates, which consist of complementary pairs of NMOS and PMOS transistors. Here, we will discuss a CPL circuit diagram using AND and NAND gates.

Complementary Pass Transistor Logic (CPL) is a digital circuit design technique that utilizes pass transistors in a complementary manner to implement logic functions efficiently. In CPL, logic gates are constructed using transmission gates, which consist of complementary pairs of NMOS and PMOS transistors. Here, we will discuss a CPL circuit diagram using AND and NAND gates.

1. CPL AND Gate Circuit:

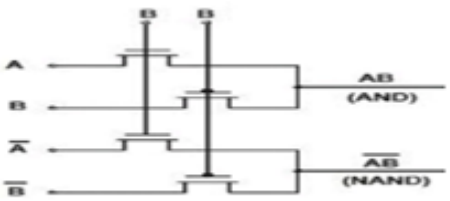
An AND gate in CPL can be implemented using transmission gates and inverters. The basic idea is to pass the inverted and non-inverted inputs through transmission gates and then perform a logical AND operation on these signals.

Let's represent the inverted input as A' and the non-inverted input as A.

- NMOS Transmission Gate: Passes signal when input is logic high.
- PMOS Transmission Gate: Passes signal when input is logic low.

2. CPL NAND Gate Circuit:

Similarly, a NAND gate in CPL can be implemented using transmission gates and inverters. In this case, we perform a logical NAND operation on the inverted and non-inverted inputs.



Let's represent the inverted input as B' and the non-inverted input as B.

Fig 3. CPL AND & NAND gate

Table 1 : Truthtable of AND & NAND

Truth table :

A	B	A.B	$\overline{AB}$
0	1	0	1
1	1	1	0
0	0	0	1
1	0	0	1

The main advantages of CPL include:
• Reduced transistor count
• High speed operation
• Low power consumption
• Efficient implementation of XOR logic
However, CPL circuits may experience threshold voltage drop and require swing restoration techniques.

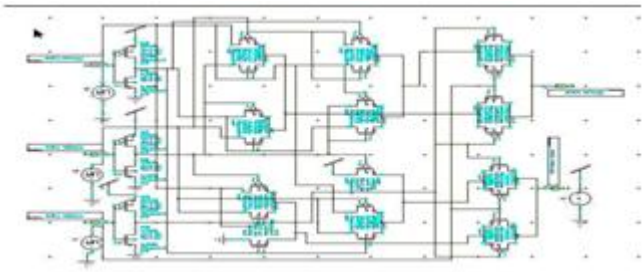


Fig. 2. CPL full adder Tanner schematic representation.

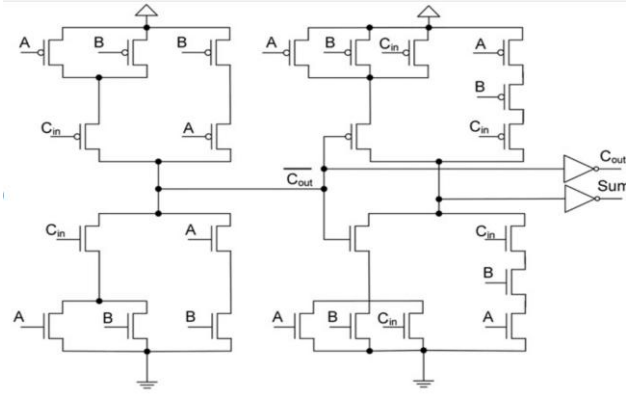
IV. CMOS FULL ADDER ARCHITECTURE

A full adder performs the addition of three input bits A, B and Cin and produces two outputs Sum and Carry. The Boolean expressions for full adder are:
In CPL based design, XOR gates are efficiently implemented using pass transistor logic which reduces transistor count. The proposed design utilizes XOR/XNOR and AND/OR modules to implement the full adder functionality.
Fig. 3. Conventional 28T CMOS full adder circuit.

V. SIMULATION RESULTS

The proposed CPL based full adder was simulated using **Tanner EDA tools**. The simulation results include waveform analysis and performance comparison with CMOS based designs.

Power Consumption



Circuit	CMOS	CPL
XOR	1.08×10^{-4}	0.68×10^{-4}
Full Adder	9.69×10^{-5}	4.59×10^{-5}

Transistor Count Comparison

Circuit	CMOS	CPL
XOR	14T	10T
Full Adder	28T	24T

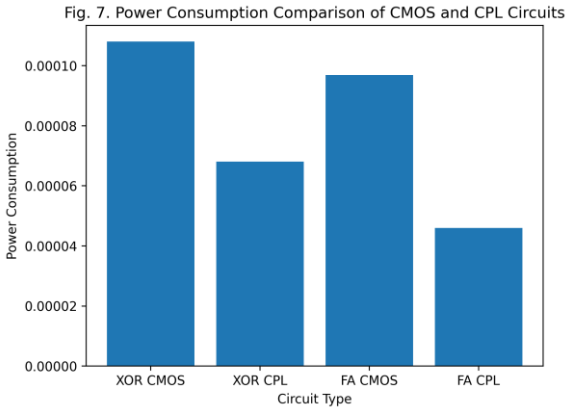


Fig. 4. Power consumption comparison between CMOS and CPL circuits.

VI. CONCLUSION

This paper presented a modified full swing restored CPL based full adder for low power applications. The proposed design reduces transistor count and power consumption compared to conventional CMOS full adders. Simulation results show that the CPL based design improves speed and energy efficiency. Therefore, the proposed full adder is suitable for high performance and low power VLSI applications such as processors, digital signal processing systems, and arithmetic units.

REFERENCES

[1] Goel S., Kumar A., Bayoumi M., Design of robust energy efficient full adders, IEEE Transactions on VLSI Systems, 2006.
[2] Borkar S., Design challenges of technology scaling, IEEE Micro, 1999.
[3] Chandrakasan A., Brodersen R., Minimizing power consumption in CMOS circuits, Proceedings of the IEEE, 1995.
[4] Roy K., Prasad S., Low Power CMOS VLSI Circuit Design, Wiley, 2000.
[5] B. Razavi, Design of Analog CMOS Integrated Circuits. New York, NY, USA: McGraw-Hill, 2001.
[6] K. Navi, O. Kavehei, M. Rouholamini, A. Sahafi, S. Mehrabi, and N. Dadkhah, “Low-power and high-speed full-adder cells based on XOR–XNOR gates,” Microelectronics Journal, vol. 40, no. 1, pp. 126–130, Jan. 2009.
[7] S. Goel, M. Elgamel, M. A. Bayoumi, and Y. Hanafy, “Design methodologies for high-performance noise-tolerant XOR–XNOR circuits,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 4, pp. 867–878, Apr. 2006.
[8] J. Wang, S. Fang, and W. Feng, “New efficient designs for XOR and XNOR functions on the transistor level,” *IEEE Journal of Solid-State Circuits*, vol. 29, no. 7, pp. 780–786, Jul. 1994.