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Review of modelling of surface potential for channel and gate engineered MOSFETs in subthreshold regime

[1]Swapnadip De, [2]Debasmita Ghosh, [3]Debjani Satpati

[1]Associate Professor, [2]Student, [3]Student

[1]Department of Electronics and Communication Engineering

[1]Meghnad Saha Institute of Technology, Kolkata, India

Abstract : In this work a review of modelling of subthreshold surface potential for short channel, LAC,Double halo and Double gate MOSFETs are carried out. The models are plotted using MATLAB. It is found that the results tally well with the models and simulation results from existing literatures.

Index Terms – Subthreshold surface potential, channel engineering, gate engineering

I. INTRODUCTION

It is found that the channel and gate engineering techniques, as well as Double gate MOSFETs suppress short channel effects effectively as in [1]-[6]. Here for double material gate two laterally contacted materials of different work functions are used. In the channel of MOSFET two different materials M_1 and M_2 with lengths L_1 and L_2, and with work functions are Φ_1 and Φ_2 respectively, contacted laterally are used as the gate. The overall effective channel length $L=L_1+L_2$ is defined as the distance from the source-channel metallurgical junction to the drain-channel metallurgical junction. The work function of the metal gate 1 (M_1) is greater than that of metal gate 2 (M_2), that is, $\Phi_1 > \Phi_2$ for n-channel MOSFET. This gives rise to a step change of the surface potential profile at the point where M_1 and M_2 are contacted. The potential distribution introduces an additional peak field inside the channel resulting in a reduction of the field at the drain end. Thus the device immunity to the hot carrier effect is also increased.

An analytical model for the sub thershold surface potential in a short channel MOS transistor is developed by solving a pseudo-2D Poisson's equation, formulated by applying Gauss's law around a rectangular box in the channel depletion region. This model uses a physcially based non-uniform depletion layer depth along the channel incorporating the role of channel length (L) and junction depth (x_j) , substrate doping (N_a), oxide thickness (t_{ox}), and bias voltages in determining the surface potential.

II Model description

Only the 2-D analysis in the channel can provide accurate results. The analytical solution of the 2-D Possoin's equation is futher very complicated.Here Gauss's Law is applied to a recatngular box covering the total depletion layer depth. For Double gate MOSFET, At a given x, such an elementary Gaussian surface of length Δx covering the entire depletion width y_d is shown in Fig 1.1 where W is the gate width. Since the region outside the depletion layer is neutral, the vertical field E_{y2} on the bottom or back side and on the top or front side surface, E_{y1} along the y direction is not zero here. So E_{y1} and E_{y2} can be obtained from the potential balanced equation:

$V_{gbf} = V_{fbf} + \psi_s + \psi_{ox}$ and the bottom side $V_{gbb} = V_{fbb} + \psi_s + \psi_{ox}$ where ψ_s= Surface potential drop from surface to bulk outside the depletion region, ψ_{ox} = The potential drop across the oxide. V_{gbf} is the front gate bias voltage, V_{gbb} is the back gate bias voltage and V_{fbf} and V_{fbb} are the flat band voltage under front gate and back gate.

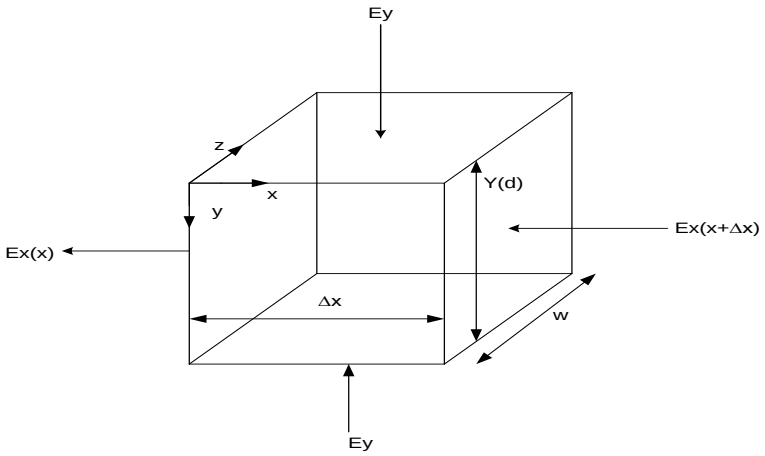

Fig:1.1: Gaussian surface

The flux line terminating on the interface charge per unit area Q_0 will not contribute to the same since it is modeled as the effective interface charge which resides on the oxide side of the interface. Only flux lines terminating on Qc will contribute to the same and for an oxide thickness of t_{ox}, the corresponding vertical field can be obtained as:

$$E_{y1} = \frac{V_{gbf} - V_{fbf} - \psi_s}{t_{ox}} \quad \text{and} \quad E_{y2} = \frac{V_{gbb} - V_{fbb} - \psi_s}{t_{ox}}$$

In week inversion, the inversion layer charge can be ignored. For a substrate doping of a N_a, the total depletion charge due to the ionized acceptor atoms within the Gaussian surface is given by $-q\, N_a\, \Delta x\, y_d\, W$ here q is the electronic charge. Therefore if the dielectric permittivity of the medium is ε the mobile charge carriers are ignored, then after application of Gauss's law to the said surface, we get the following equation

$$\varepsilon \oint_{surface} \vec{E}.\vec{ds} = -qN_a\, y_d\, \Delta x\, W$$

The left, right, top and bottom surface of the Gaussian box will have non-zero contribution to the left side of the integration. ε_{si} silicon and ε_{ox} SiO_2 respectively, can be expanded to

$$-\varepsilon_{ox} E_{y1}\, \Delta x\, W + \varepsilon_{ox} E_{y2}\, \Delta x\, W + \varepsilon_{si} \{-E_x(x+\Delta x)+E_x(x)\}\, y_d W = -qN_a \Delta x y_d W$$

So this equation can be written as

$$-\varepsilon_{ox} * \{ (V_{gbf}-V_{fbf}-\psi_s)/t_{ox}\}\, W + \varepsilon_{ox} * \{(V_{gbb}-V_{fbb}-\psi_s)/t_{ox}\}\, \Delta x\, W + \varepsilon_{si}\{E_x(x+\Delta x)+E_x(x)\}\, y_d W = -q\, N_a\, \Delta x\, y_d\, W$$

So , $-\varepsilon_{si} * (d^2\psi_s/dx^2) - (c_{ox}/y_d)\psi_s = qN_a - (c_{ox}/y_d)(V_{gbf}-V_{fbb}) - (c_{ox}/y_d)(V_{gbf}-V_{fbb})$

or, $-\varepsilon_{si} * (d^2\psi_s/dx^2) - (c_{ox}/y_d)\psi_s = qN_a - (c_{ox}/y_d)\, V'_{gsf} - (c_{ox}/y_d) V'_{gsb}$

or, $-\varepsilon_{si} * (d^2\psi_s/dx^2) - (c_{ox}/y_d)\psi_s = qN_a - (c_{ox}/y_d)\, (V'_{gsf} - V'_{gsb})$ (1)

Left, right, top, bottom surface of Gaussian box are non zero. But in this case E_x is directed along the negative x direction.

where $V'_{gsf} = V_{gsf} + V_{sb} - V_{fbf}$ and $V'_{gsb} = V_{gsb} + V_{sb} - V_{fbb}$

V_{gsf} / V_{gsb}= Front / back Gate to source voltage, V_{sb} =Source bias voltage,

V_{fbf} / V_{fbfb}= Front and back Flat band voltage under the front and back Gate the Mosfet.

For double metal gate MOSFET

Φ_{M1}= Work function of metal 1(M_1), Φ_{M2}= Work function of metal 2 (M_2)

Here in halo region Flat band voltage

$V_{fbp} = -(E_g/2q) - \Phi_t \ln(N_p/n_i)$, where $\Phi_t = kT/q$

Φ_t is the thermal voltage,

n_i the intrinsic carrier density ,

N_p halo doping concentration
E_g the band gap in silicon=1.1ev
Flat band voltage of P-type substrate $\Phi_{fn=}\Phi_t \ln(N_a/n_i)$,
N_a= p- type substrate doping concentration,
y_d is the depletion layer depth under the gate,

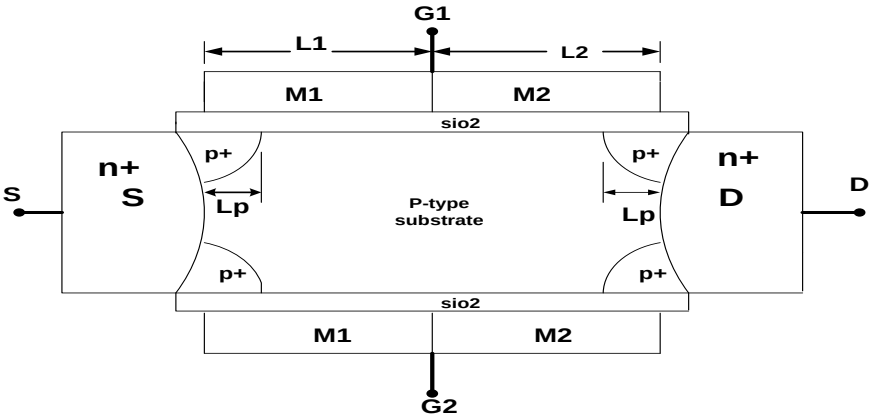

Fig: 1.2 DGDHDM MOSFET structure

For short channel Double gate double pocket double metal MOSFET , the contribution of two junction regions and for two different metal gate and two halo doping,which causes a non uniformity to y_d . so surface potential depends on depletion layer thickness which is not constant for this model. So $y_d(x)$ be modeled first for an accurate prediction of the surface potential. If the channel length is not too small and reasonable amount of voltage is applied to source and drain, $y_d(x)$ is typically varying with x . Unfortunately, the depletion layer depth around the source and drain junctions is a complex function of substrate doping, junction depth, and drain and source bias voltages. So flat band voltage under metal 1 of gate is $V_{fb1}=(\Phi_{M1}-\Phi_s)/q$, and Flat band voltage under metal 2 of gate is $V_{fb2}=(\Phi_{M2}-\Phi_s)/q$, where work function of silicon substrate is

$\Phi_s=(E_g/2q)+\Phi_f+\chi$, where χ is the electron affinity of silicon,

$C_{ox}=\varepsilon_{ox}/t_{ox}$ is the oxide capacitance per unit gate area, t_{ox} is the gate oxide thickness ε_{si} and ε_{ox} are the dielectric permittivity of Si and SiO_2 respectively.To predict Ψs accurately, an appropriate model for $y_d(x)$.If the effect of the source and drain junction depletion regions neglected, it can be expressed as

$y_d=(2\varepsilon_{si}\Psi_s/qN_a)^{1/2}$, where $\Psi_s=(\gamma/2+(\gamma^2/4+V_{gb}-V_{fb})^{1/2})^2$

is the gate-controlled sub threshold surface potential for a long channel MOSFET, and

$\gamma=(2q\,\varepsilon_{si}N_a)^{1/2}/C_{ox}$ is the body effect co-efficient.

different y_d results ($y_{(d)1}$, $y_{(d)2,}$ $y_{(d)3,}$ $y_{(d)4}$) because of four different flat band voltage V_{fbp1} , $V_{fb1,}$ V_{fb2} and V_{fbp2} due to M_1 ,M_2 and both side halo region but difference of flat band voltage under the Front gate and Back gate. Considering the typical variation of $y_d(x)$ with x near the source and drain junctions, we use a physically based simple and approximate model for it as $y_d(x)=(ax+b)^2$. The channel is then divided into six regions, and in all the regions, the depletion layer depth is modeled as

$y_d(x)=(ax+b)^2$ in equation 1.

so $$(ax+b)^2\frac{d^2\Psi_s}{dx^2}-\frac{c_{ox}}{\varepsilon_{ci}}\Psi_s=\frac{qN_a}{\varepsilon_{ci}}(ax+b)^2-\frac{c_{ox}}{\varepsilon_{ci}}(V'_{gsf}-V'_{gsb}) \qquad (2)$$

Based on the channel length, pocket length, doping concentration, and applied voltages, two cases for the six regions are required to be considered under the boundary values of potential

At $x_1=0$ position of the channel length voltage $V_1=V_{bi}+V_{sb}$

At $x_7=L$, position of the channel length voltage $V_7=V_{bi}+V_{db}$

Where V_{bi}= Built in potential, $V_{bi}=(E_g/2q)+\Phi_{fp}$, and when $\Phi_{fbp}=\Phi_t\ln(N_p/n_i)$, Fermi potential of p-type substrate , $\Phi_t=kT/q$ the thermal voltage, n_i is the intrinsic carrier density, and V_{ds} is the drain-to-source bias.

Using the substitution t = ln (ax+b), dt/dx=a/(ax+b) .we can solve (equ^n 1) for Ψ_s as given below for the various regions, D=d/dt, so we can write

$$(ax+b)^2\frac{d^2\Psi_s}{dx^2}=a^2D(D-1)\Psi \qquad (3)$$

So, $d= \sqrt{(1/2)^2 + (C_{ox}/ \varepsilon_{si}a^2)}$, and C_1 and c_2 are the arbitrary constant, so complementary function $CR = e^{\frac{t}{2}}\left(C_1 e^{dt} + C_2 e^{-dt}\right)$, $\beta= qN_a/ (2 \varepsilon_{si}a^2 – C_{ox})$, so particular integral is $PI = \beta e^{2t} + (V'_{gsf} - V'_{gsb})$

So for Front gate flat band voltage under halo and material 1 is $V_{fbpf1}=V_{fbfp}-V_{fbf1}$,

for back gate flat band voltage under halo and material 1 is $V_{fbpb1}=V_{fbbp}-V_{fbb1}$,

for Front gate flat band voltage under halo and material 2 is $V_{fbpf2}=V_{fbfp}-V_{fbf2}$,

for back gate flat band voltage under halo and material 2 is $V_{fbpb2}=V_{fbbp}-V_{fbb2}$

IV. RESULTS AND DISCUSSION

In this work subthreshold surface potential of short channel and Channel and gate engineered Double Gate MOSFETs are obtained using MATLAB.

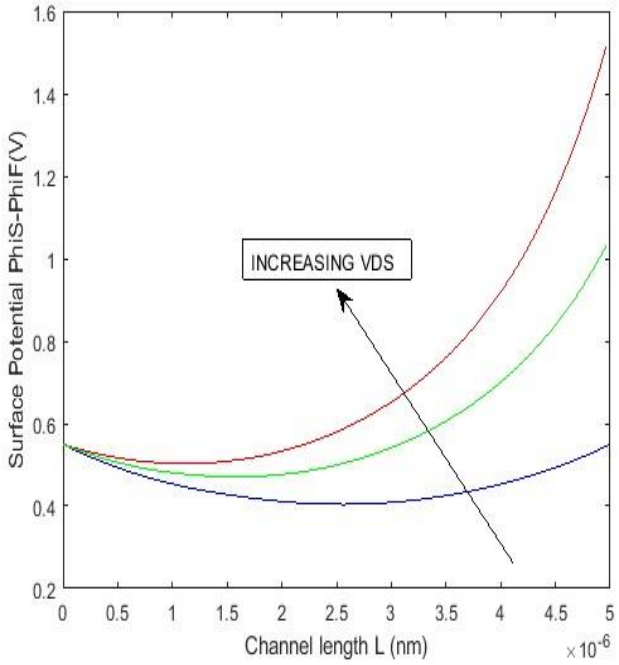

Fig:1.3(a)

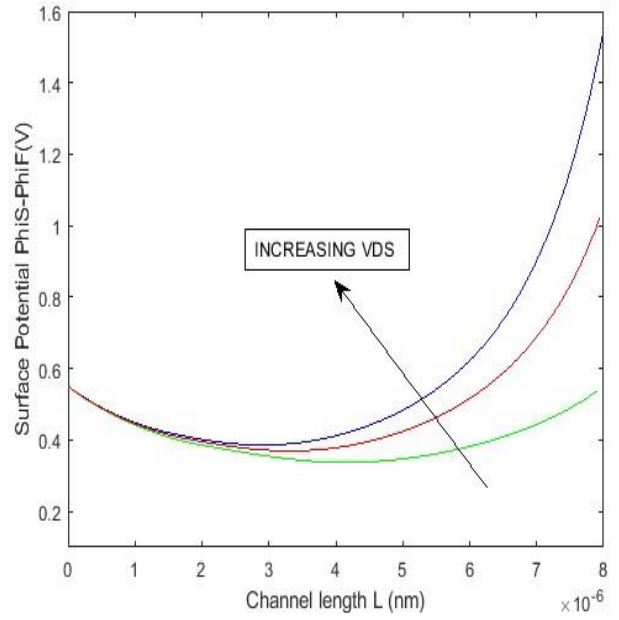

Fig:1.3(b)

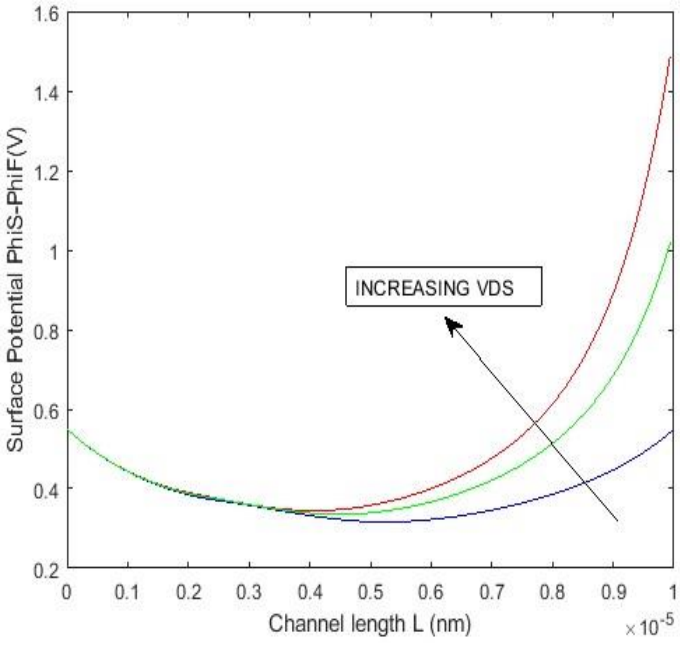

Fig: 1.3(c)

Fig 1.3(a,b,c) Plot of subthreshold surface potential vs channel length for L=50 ,80 and 100nm considering Na = 4*10^17 cm^-3

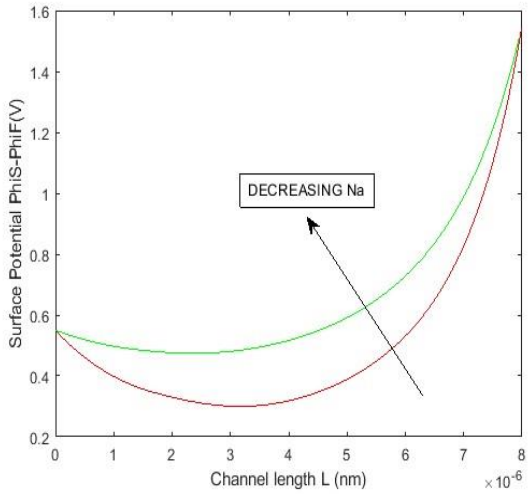

Fig 1.4 Plot of surface potential vs channel length considering Na=10^18 and 2*10^17 cm^-3

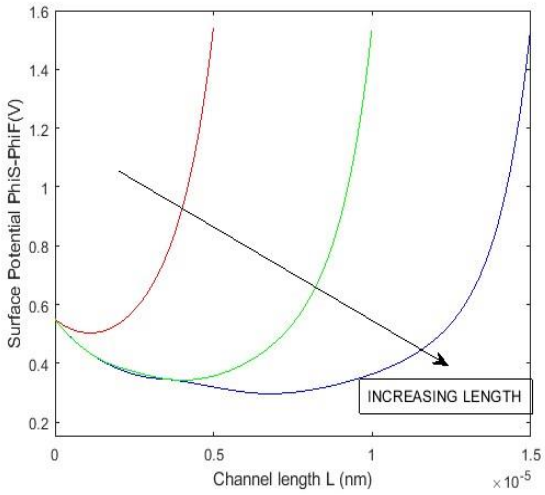

Fig 1.5 Plot of surface potential vs channel length considering L=50 ,100,150 nm

The DGDMDH structure uses a relatively lower doped substrate than halo region in the channel. The high Work function near the source leads to more rapid acceleration of carriers in the channel and the low Work function near the drain leads to reduction of peak electric field at the drain side.

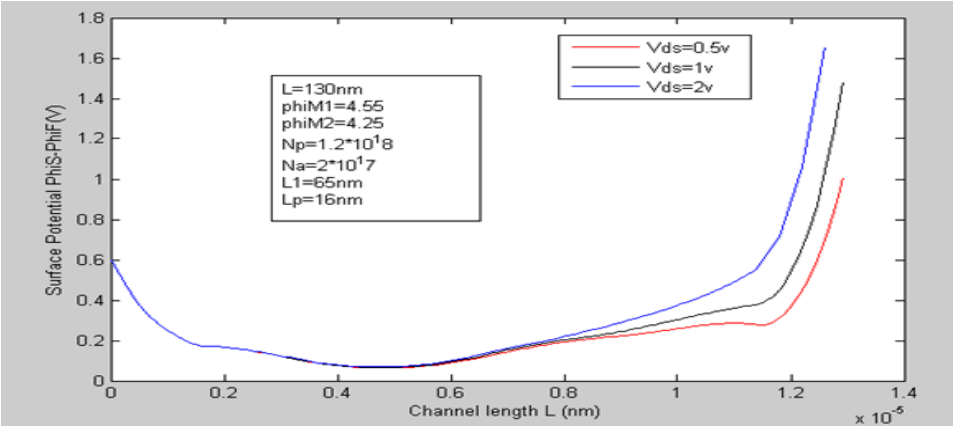

Fig:1.6 (a) Surface potential v/s channel length plot for V_{ds} =0.5V, 1V, 2V in L= 130 nm

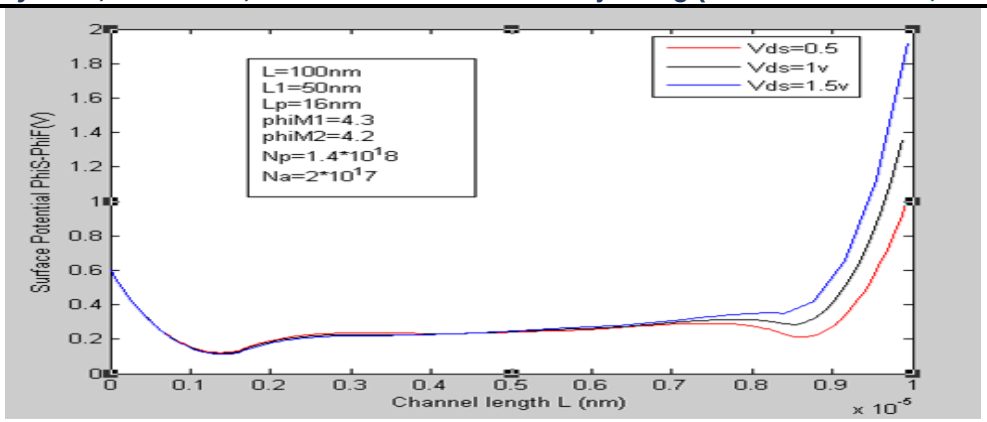

Fig :1.6 (b) Surface potential v/s channel length plot for V_{ds} = 0.5V, 1V and 1.5V in L=100 nm

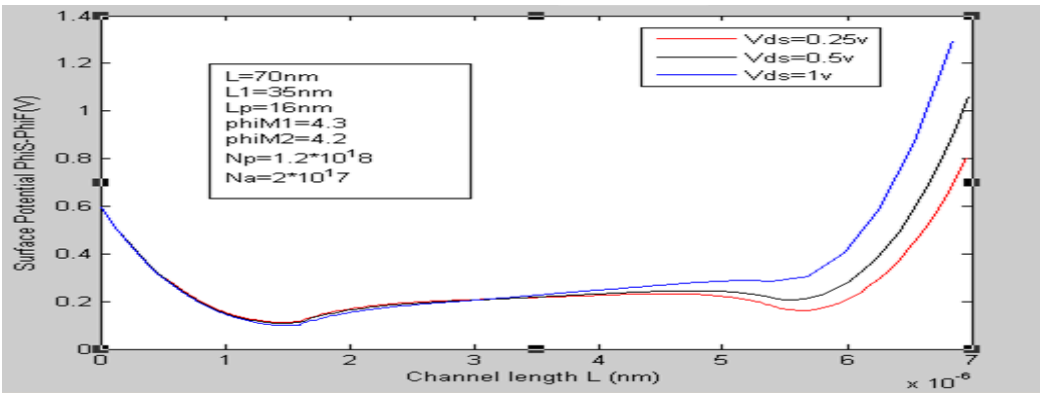

Fig:1.6(c) Surface potential v/s channel length plot for V_{ds} =0.25V, 0.5V, 1V in L=70 nm

It is seen that as the drain-to-source voltage is increased, then the depletion depth increases and the inversion charge increases and the

V. CONCLUSION

The surface potential is the most important parameter which needs to be found for any device. In this thesis Double Gate Dual Material Double Halo structure, combining the channel and gate engineering technique to double gate MOSFET is proposed. Some existing literature used simulation to show that Single Halo Dual Material Double Gate structure suppresses short channel effects more effectively than halo or DMG MOSFETs. An analytical expression of surface potential in sub threshold region is formulated by applying Gauss's law to a rectangular box in the channel, covering the entire depletion depth. This method eliminates the need of solving complex Poisson's equation in the channel.

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