GDI implementation of Low Power Modified Booth Multiplier

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Abstract

The basic operations used in any circuit are addition and multiplication as all the other operations such as subtraction, filtering and convolution are performed by the help of these operations only. In digital signal processing the main task is to perform the inner product, sampling and convolution which is mainly performed by the help of multiplier only. Hence to overcome a problem of problem of delay and power consumption the use of digital multiplier instead of analog multiplier takes place. This paper introduced a low power booth multiplier. In a booth multiplier the multiplication take place with the help of shifting, addition and partial product. The booth multiplier consists of a three section decoder, partial product generation unit and adder circuit. The booth multiplier recodes the input value to the booth equivalent value to reduce the switching activity in a circuit. This paper consist a booth multiplier design using a power reduction techniques called FINFET and the result is compared with the result of GDI and CMOS. The implementation of a booth multiplier takes place using a cadence virtuoso. The result obtained is compared in term of average power and noise by the help of various reduction techniques in 16nm technique. The input voltage in this paper varies from 0.5 to 0.7 V

Keywords: Booth decoder, half adder, full adder, partial generating unit, AND gate, OR gate, XOR gate, 2-bit binary encoder, CMOS and NAND gate

Introduction

There are different other power reduction techniques, compared to the other techniques GDI provides lowest power dissipation. For lower power circuit the Gate Diffusion Input technique is used. When lowest power dissipation in GDI implementation occurs it reduces the logic switching and static power dissipation. The main advantage of the GDI technique is that it uses the less number of transistor compared to the CMOS, so the reduction in noise and power dissipation takes place easily. GDI consists basic cells they are PMOS and CMOS with four terminals drain, gate, source and body. The booth multiplier performs the low reduction power and high speed operation. And the booth multiplier is the combination of both shifting arithmetic and repeated addition. In GDI technique the booth multiplier consists three sections they are partial generating unit, adder circuit and encoder.

Literature survey

1. Nilanjan Banerjee [2] had proposed architecture support for displayed approximate programming and diminishing benefits from technology scaling on the one hand, and projected growth in computing demand from future workloads on the other, leads to a need for new sources of computing efficiency. However, this new scaling paradigm is not without its own challenges – most applications demonstrate saturating, if not diminishing, performance with increasing core counts, due to well-known bottlenecks such as serial computations, synchronization, global communication and off-chip memory bandwidth [3], [4]. These challenges are pushing designers to look for alternate avenues to improve the capabilities of computing platforms.

2. Yi-Ming Yang [3] proposed a traditional n-bit adders provide accurate results, but the lower bound of their critical path delay. He worked on Low-power digital signal processing using approximate adders.. The experimental results show that the proposed carry speculative adder (CSPA) achieves a 26.59% delay reduction, a 14.06% area reduction, and a 19.03% power consumption reduction compared to the corresponding values for an existing speculative carry-select adder.

3 Ning Zhu, W.L.Goh and K.S.Yeo [4] are worked based on an enhanced Low-Power high-speed Adder for Error-Tolerant application. In that they proposed the trade between power consumption and the speed performance has become a major design consideration when the devices approach the sub 100nm regime. It especially critical dealing with large data set, where by the system is degraded in terms of power and speed. They concerned a novel on low-power and high speed Error-Tolerant Adder Type IV design called ETAIV.ETAII splits the entire carry propagation chain into M short paths where by each of the carry signals if the short paths are propagated concurrently.

4. Gupta et al. proposed approximate mirror adder design [5]. It required a large number of transistors and also increased the power consumption and delay. Approximate adders are the building block for any arithmetic circuit used in inexact computing. Approximate adders are derived from accurate adders based on various approximations which have incorrect outputs for sum (S) and carry out (Cout) for some input combinations. Nanu *et al*. designed approximate adder using complementary pass transistor logic (CPL) which offer advantage in
terms of power and delay [8].He worked on design of Low Power, Area Efficient and High Speed Approximate Adders for Inexact Computing has several applications.

5. Kyung-Ju-Cho, Kwang-Chul-Jeel, Jin-Cyun-Chung and Keshub they presents the Error compensation method for a modified Booth-fixed multiplier which receives a W-Bit input and produces a W-Bit products. It is too efficiently compensate for the quantisation error, and Booth encoder outputs are used for the generation of the error compensation.

Here, we apply the proposed fixed-width multiplier to low pass finite-impluse response (FIR) filter implementation. This filter coefficients are obtained using the Remez exchange algorithm. By this simulation, the performance of the proposed method is much then the fixed-width modified Booth multiplier design method.

Implementation of 4x4 multiplier

This approach is to design the low power 4x4 multiplier with less no. of transistor in the circuit. It has the basic building blocks which consists of AND gate, half adder and Full adder. In this implementation each bit is multiplied with multiplicand and multipFig. Block diagram 4x4 multiplier using AND gate, half adder and full adder

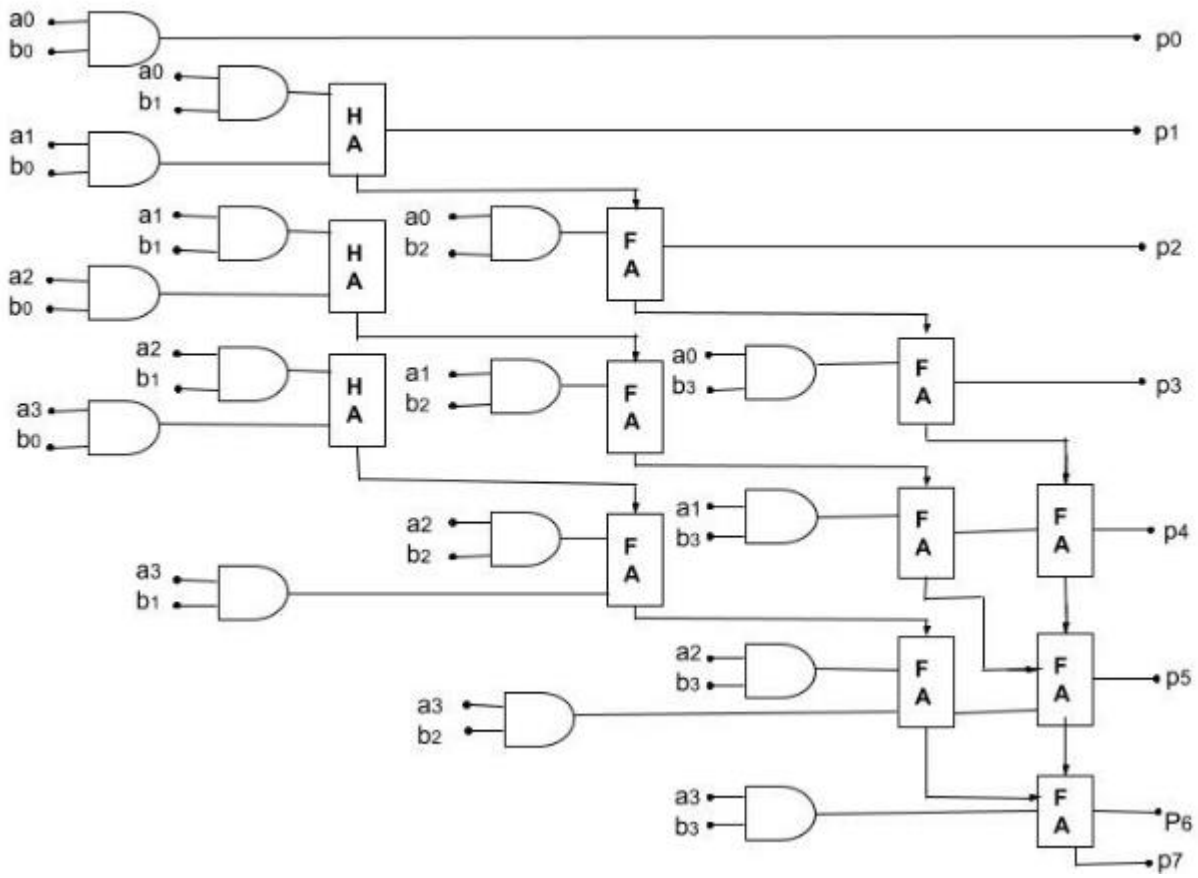

Fig .Block diagram of 4x4 multiplier using AND gate, half adder and full adder

GDI AND gate schematic

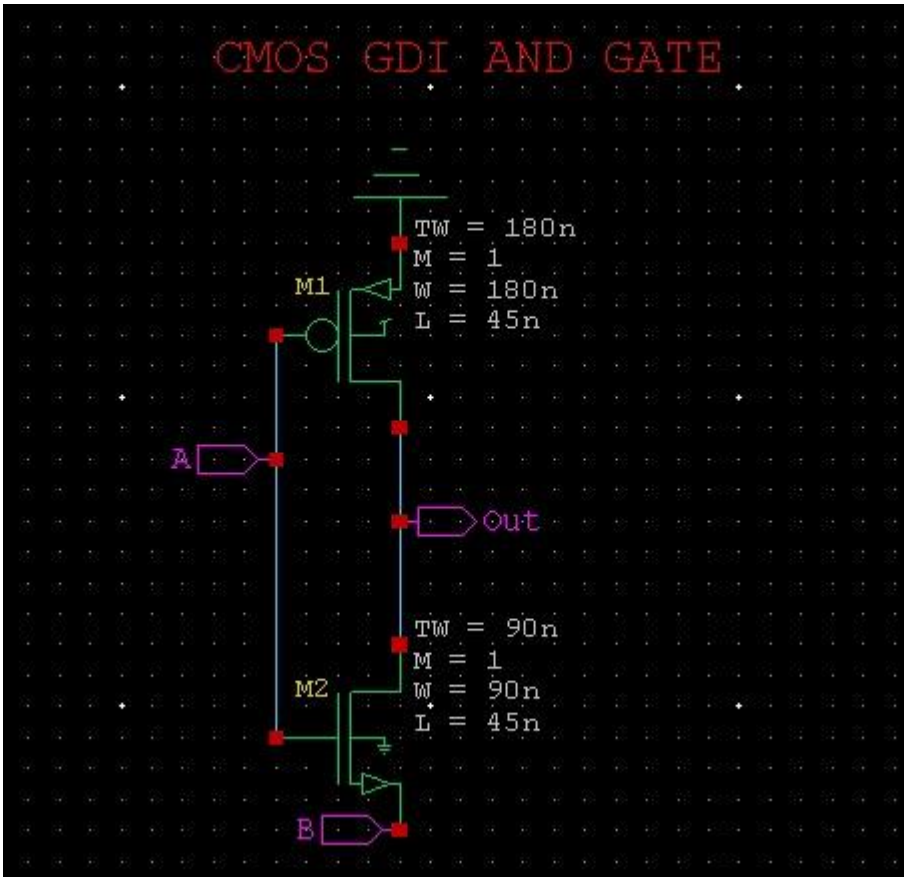

Figure1.GDI AND gate schematic

Schematic Explanation

The above schematic represents the GDI AND gate.It has two inputs which are represented as A,B and one output which is represented as Out.The above schematic has one PMOS which is represented as M1 and one NMOS that is represented as M2.Here PMOS is connected to ground and NMOS is connected to input B.Input A is connected to both the PMOS and NMOS and the output is taken from the common point of PMOS and NMOS.

Truth Table 1a.GDI AND gate

A	B	c
0	0	0
0	1	0
1	0	0
1	1	1

Simulation of GDI AND gate

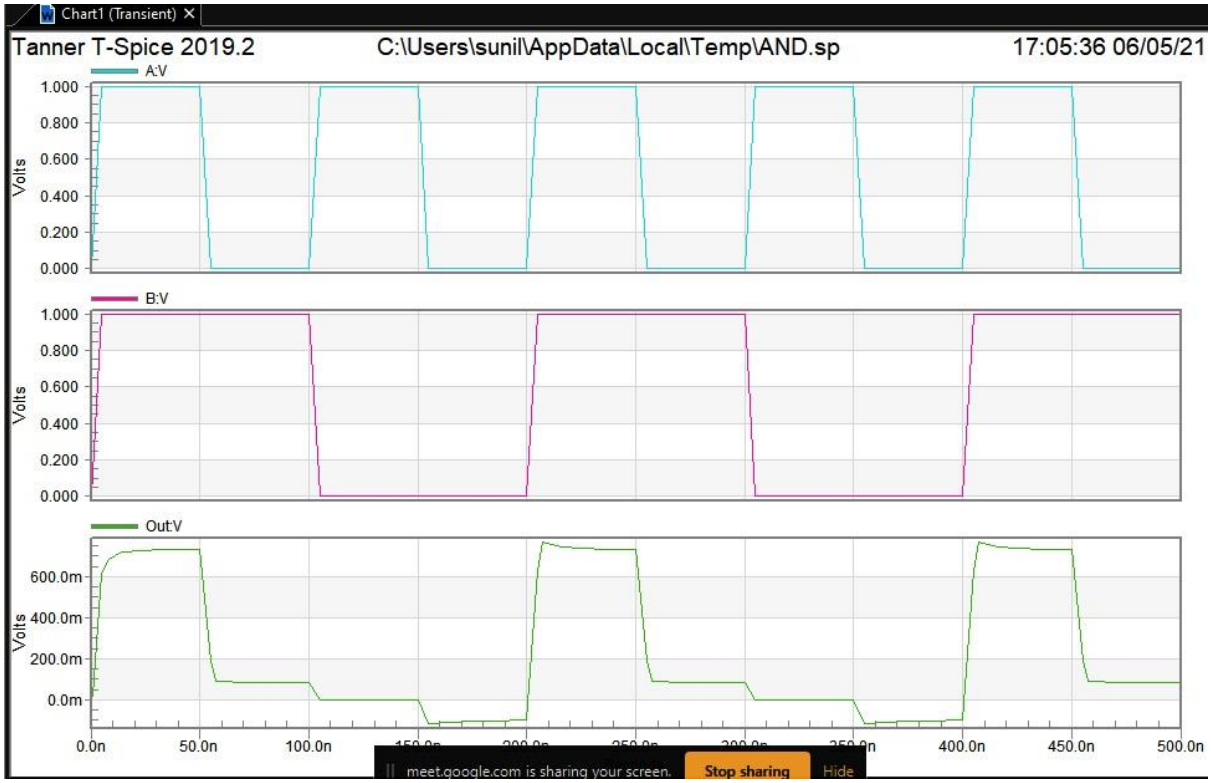

Figure 1b.simulation of GDI AND gate

Simulation Explanation

The above simulation represents about the GDI AND gate.In the above simulation inputs are A,B and output is Out. It is clearly states that if any one of the input is low,the output is low.In the above simulation the input A is high ,B is high and Out is high from 0ns to 50ns and later the input A is changing its state for every 50 ns.Input B is changing its state for every 100ns and Out is changing based the inputs of A and B.Out is high when both the inputs are high that is clearly observed in the above simulation.

GDI OR gate schematic

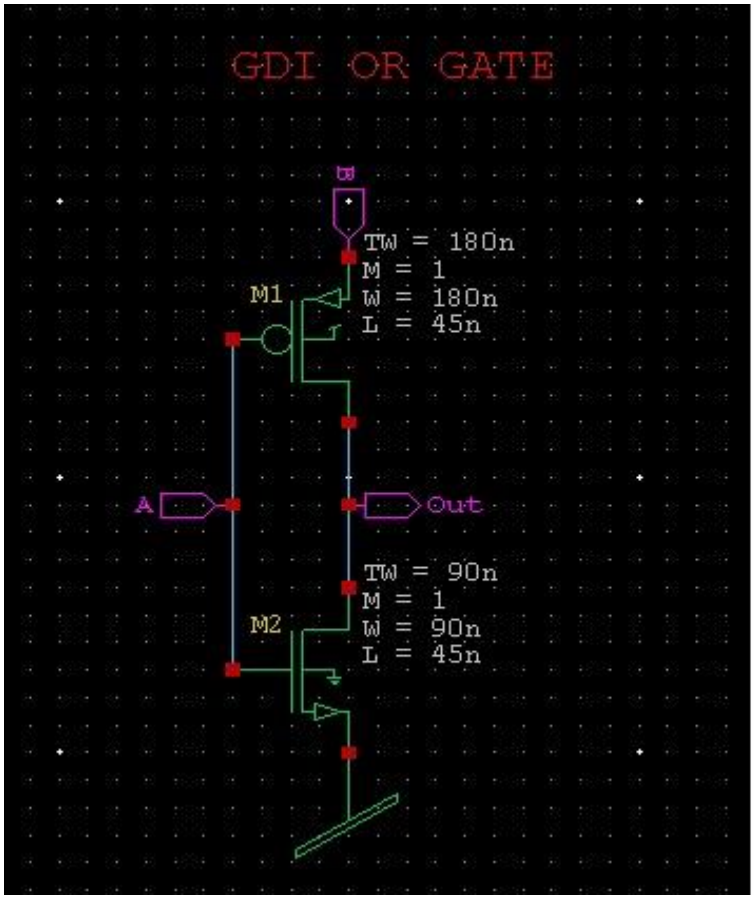

Figure2.GDI OR gate schematic

Schematic Explanation

The above schematic represents the GDI OR gate.It has two inputs which are represented as A,B and one output which is represented as Out.The above schematic has one PMOS which is represented as M1 and one NMOS which is represented as M2.Here PMOS is connected to input B and NMOS is connected to VDD.Input A is connected to both the PMOS and NMOS and the output is taken from the common point of PMOS and NMOS.

Truth Table2a.GDI OR gate

A	B	C
0	0	0
0	1	1
1	**0**	1
1	1	1

Figure 1. Basic OR gate test bench

Simulation of GDI OR gate

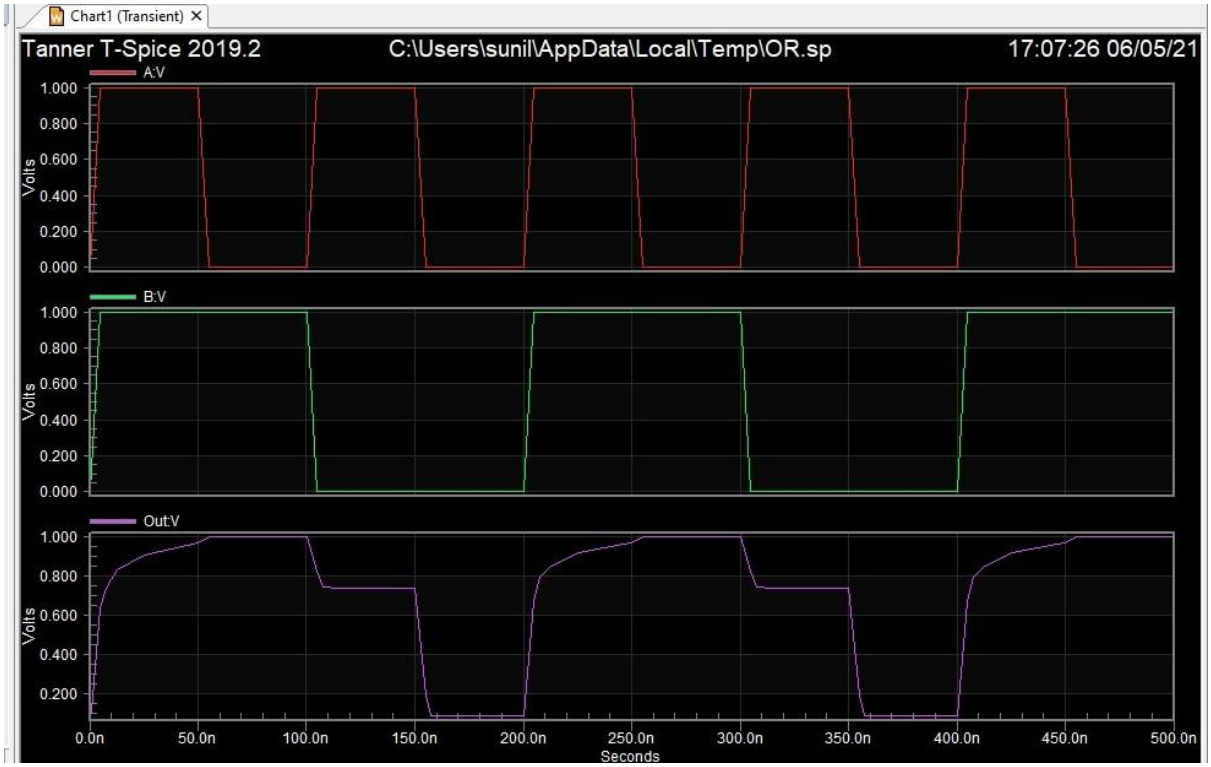

Figure 2b.simulation of GDI OR gate

Simulation explanation

The above simulation represents about the GDI OR gate.In the above simulation inputs are A,B and output is Out. It is clearly states that if any one of the input is high,the output is high. In the above simulation the input A is high ,B is high and Out is high from 0ns to 50ns and later the input A is changing its state for every 50 ns.Input B is changing its state for every 100ns and Out is changing based the inputs of A and B.Out is high when any one of the input is high that is clearly observed in the above simulation.

GDI XOR gate schematic

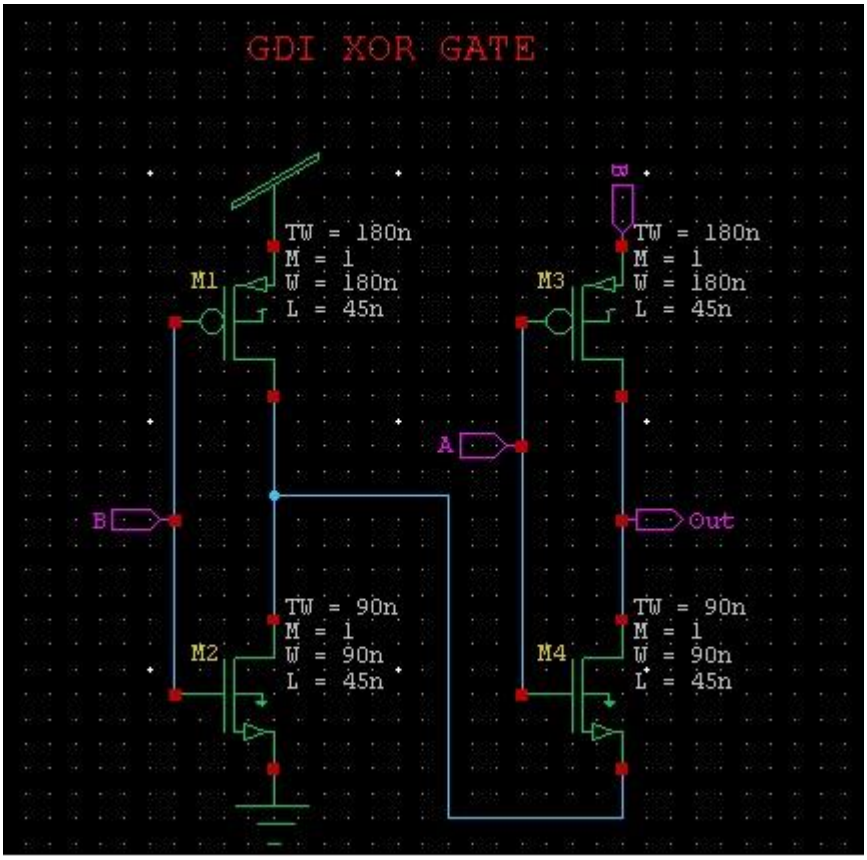

Figure3.GDI XOR gate schematic

Schematic Explanation

The above schematic represents the GDI XOR gate.It has two inputs which are represented as A,B and one output which is represented as Out.The above schematic has two PMOS and two NMOS which are represented as M1,M2,M3 and M4 respctively.Input B is connected to M1 and M2 where M1 is connected to Vdd and M2 is connected to ground.The output from the common point of M1 and M2 is connected to M4 and the input A is connected to M3, M4 where M3 is connected to input B.Out is taken from the common point of M3 .

Truth Table 3a.GDI XOR gate

A	B	Out
0	0	0
0	1	1
1	0	1
1	1	0

Simulation of GDI XOR gate

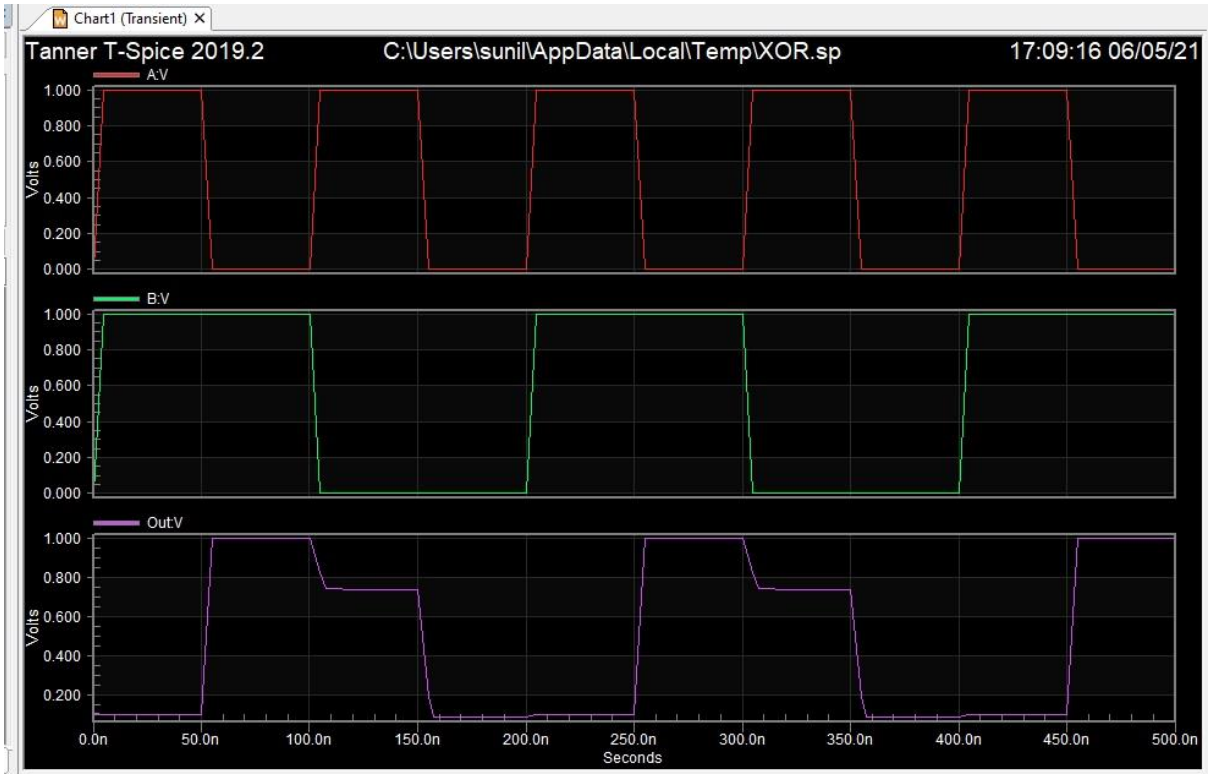

Figure3b.Simulation of GDI XOR gate

Simulation Explanation

The above simulation represents about the GDI XOR gate.In the above simulation inputs are A,B and output is Out. It is clearly states that if both the inputs are same then the out is low.In the above simulation the input A is high ,B is high and Out is low from 0ns to 50ns and later the input A is changing its state for every 50 ns.Input B is changing its state for every 100ns and Out is changing based the inputs of A and B.Out is high if one input is high and another input is low which is clearly observed in above simulation.

Schematic of GDI Full Adder

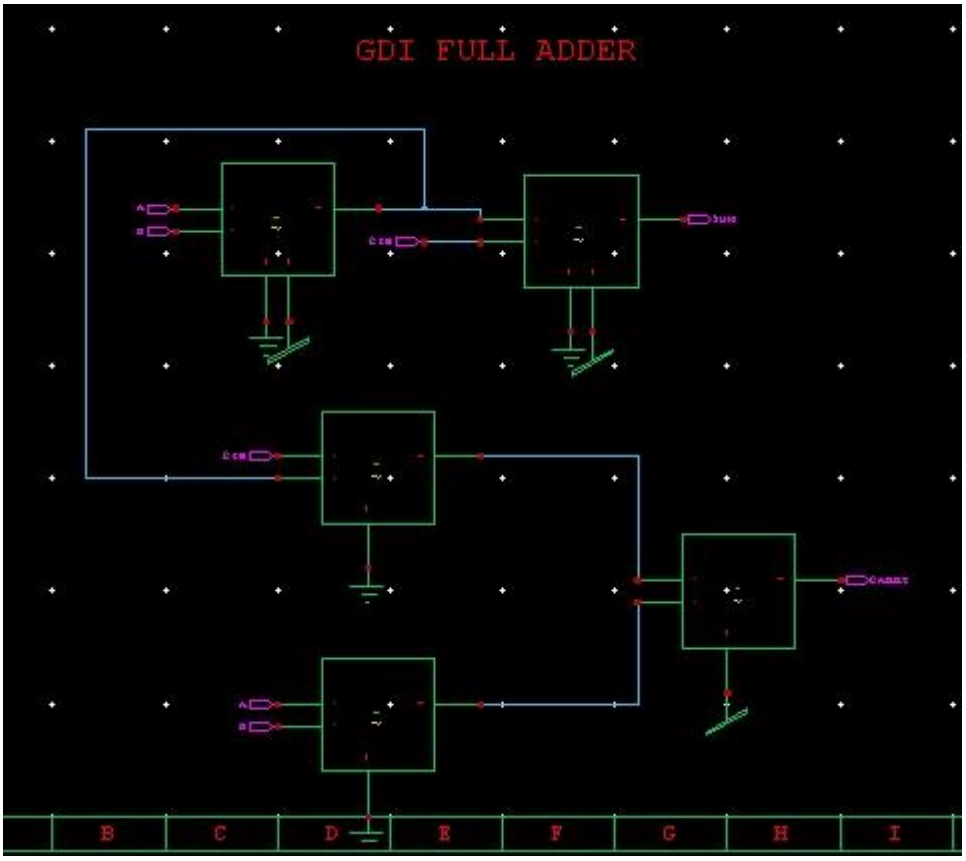

Figure4.Schematic of GDI Full Adder

Schematic Explanation

The above schematic represents the GDI Full Adder.It has three inputs which are represented as A,B,cin and two output which are represented as sum and carry.The above schematic has two XOR gates,two AND gates and one OR gate.Inputs A AND Bare connected to XOR gate1,AND gate2,the output of the XOR1 is connected to XOR gate 2 along with the input cin and the output of the XOR gate2 is sum.The output of XOR1 is connected to AND gate1 along with the input cin and the outputs of AND gate1 and AND gate 2 is connected to OR gate.The output of the OR gate is carry.Eah gates are individually connected to ground and VDD.

Truth Table 4a.GDI Full Adder

Inputs			Outputs	
a	B	c	sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1`	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Simulation of GDI Full Adder

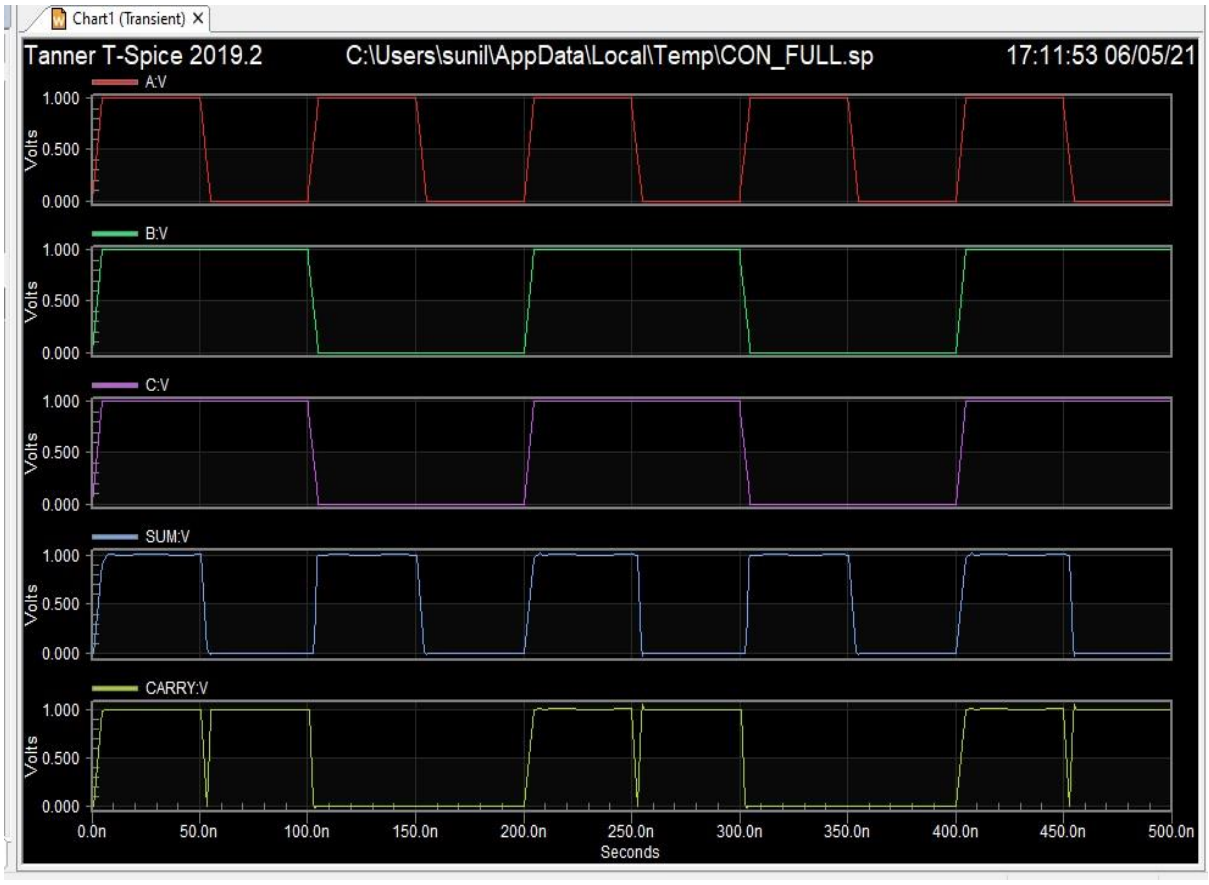

Figure4b.Simulation of GDI Full Adder

Simulation Explanation

The above simulation represents about the GDI Full Adder.In the above simulation has three inputs which are represented as A,B and C and it has two outputs which are represented as sum and carry.In the Full Adder if the three inputs are high then outputs are high.In the above simulation inputs A,B and C is high and the output sum and carry is high.Input A is changing its stat for every 50ns,input B and C are changing its state for every 100ns.The output sum is changing its state for every 50ns and the output carry is changing its state for every 100ns in which the output carry is increasing and decreasing twice in every 100ns which is clearly observed in above simulation.

Results

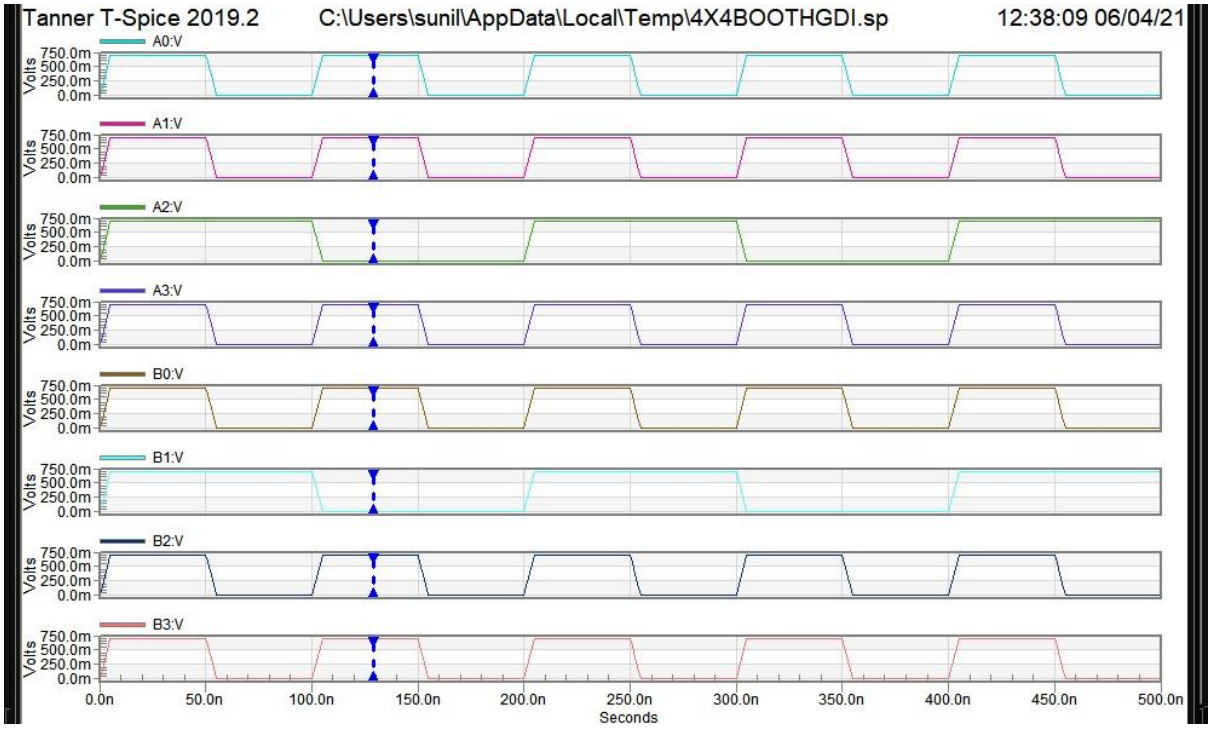

Fig. Input graph of 4x4 multiplier using AND gate, Half adder and full add

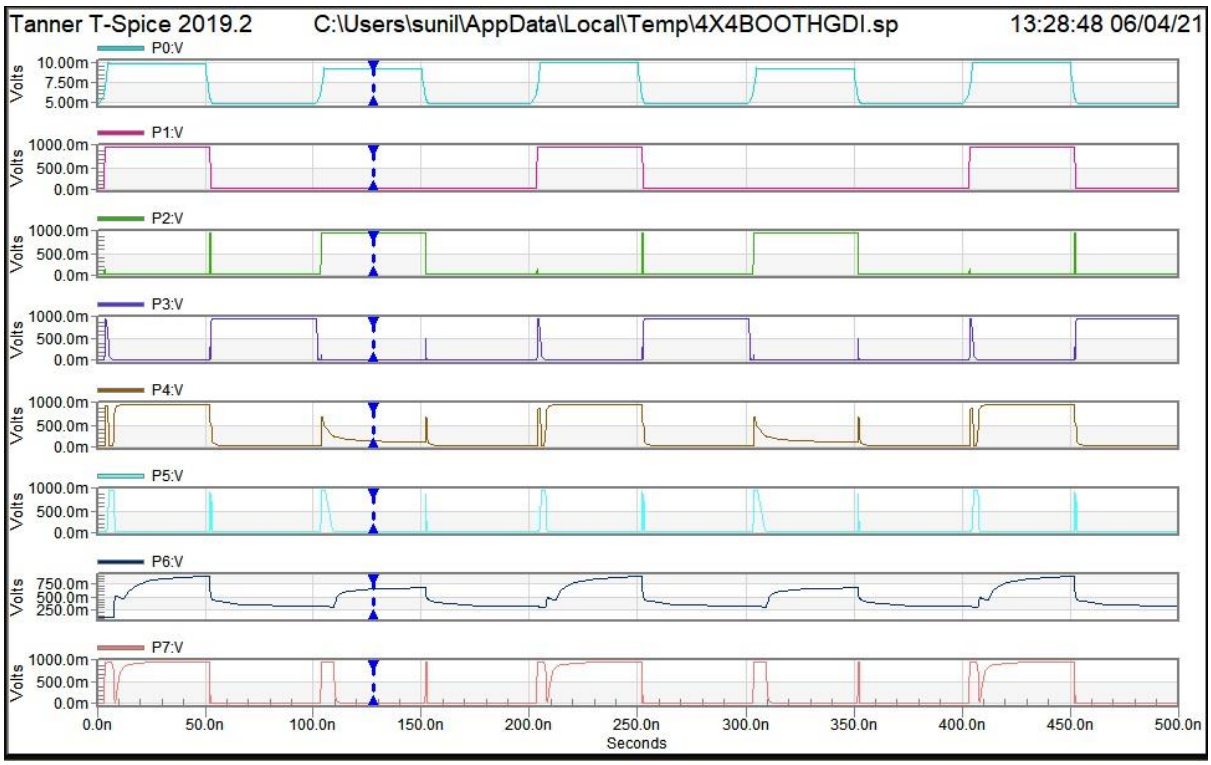

Fig. Output graph of 4x4 multiplier using AND gate, half adder and full adder

Conclusion

A modified booth multiplier implemented using CMOS and GDI technique in 45 nm using a tool cadence virtuoso. With the help of output value we conclude that the GDI technique is better than the CMOS technique in terms of power consumption and noise, as it reduces the switching of output value with the sudden change in inputs value also the area reduce with the reduction in transistor used in a circuit.

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