DESIGN AND ANALYSIS OF DIFFERENT SRAM CELL TOPOLOGIES USING CMOS AND FINFET TECHNOLOGIES

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Abstract: With the advancement of new technologies in industries, there is a requirement for low-power and high-performing circuits. SRAM efficiency can be improved by utilizing developing technologies. Complementary Metal Oxide Semiconductor (CMOS) based SRAM cells face the problems of high power and an increase in delay (read delay and write delay), which affect their performance badly. The butterfly curve shows the analysis for the static noise margin (SNM) parameter and distinguished as HSNM (Hold), RSNM (Read), and WSNM (Write). Replacing Fin Field Effect Transistor (FinFET) technology instead of CMOS technology gives a better performance because of its low power, delay, and SNM. In this project, the topologies used are 4T, 6T, 9T, and 14T SRAM cells. The parameters performed are the delay, power, and SNM. The software used to perform the parameters is Cadence Virtuoso Software. The technologies used are CMOS technology (45nm and 90nm) and FinFET technology (7nm and 16nm Predictive Technology Model – Multi-Gate (PTM-MG)). Here we have shown the schematic and results of the 9T SRAM cell in 45nm CMOS and 7nm FinFET technologies. A comparison of the CMOS and FinFET results shows that FinFET based SRAM cells perform better operations than CMOS based SRAM cells.

Index Terms - SRAM, CMOS, FinFET, Read Delay, Write Delay, Power, SNM.

I. INTRODUCTION

In the present world, based on ITRS, more than 85% to 90% of the chip area is engaged by VLSI. Our world is being taken over by Virtually Integrated Circuits. Digital appliances are indissoluble parts of the structure of today’s life scenario. The handheld devices require RAM as the major component.

SRAM is one of the best RAMs. The SRAM cell plays a prominent role in high-performance memory devices. CMOS is believed to be the best option for SRAM. Because of CMOS forceful scaling, its execution reduced due to short channel effect (SCE). FinFET technology is one of the most popular alternatives to CMOS technology. The FinFET circuits have considerably quicker reverse times and excess current density than CMOS devices. Due to its magnificent electrostatic properties and ease of fabrication, FinFET has been featured as a successful candidate for further increasing the technology to the nanoscale regime for its magnificent electrostatic properties and ease of fabrication. CMOS is a planar device where the gate gets controlled in one direction, while FinFET is a non-planar device where the gate is wrapped all around the directions and gives superb gate control. The FinFET is multi-gate structure, which is a 3D fork-shaped like a fish fin. Since the FinFET technology process is similar to CMOS technology, it is technically easier to design and analyse the circuits. So, FinFET technologies have been utilised by the VLSI companies in the manufacturing of small-size ICs.

This paper provides the design and analysis of 4T, 6T, 9T, and 14T SRAM cell topologies using (45nm and 90nm) CMOS technologies and (7nm and 16nm) FinFET technologies. The software used to perform the analysis is Cadence Virtuoso Software. Various parameters like read delay, write delay, power, and SNM (hold, read and write operations) are analyzed. The performance of both the technologies shows that FinFET based SRAM is much faster and better when compared to CMOS based SRAM.
II. LITERATURE SURVEY

Deepak Mittal et.al. [1] proposed different SRAM cell topologies using 90nm CMOS technology. This implementation is done through Cadence Virtuoso software. They have observed that 7-transistor SRAM cells have a less read power, 9-transistor SRAM cells have a minimum write delay, and power in 8-transistor SRAM cells is decreased by 44%. The WSNM of an 8-transistor SRAM cell is double than that of a 6-transistor SRAM cell.

Ajay Gaadhe et.al. [2] proposed using 130nm and 90nm MOSFET technology to design different topologies of SRAM cells. The analysis of SNM was implemented in an HSpice. They observed that the RSNM of a 10-transistor SRAM cell at 90nm is increased by 208%, the WSNM by 23.6% compared to a 90nm 6-transistor SRAM cell, and the overall stability of a 10T SRAM cell is less as compared to other SRAM topologies. The RSNM and WSNM of 10-transistor SRAM cells are reduced by 24% and 11% respectively. Technology is scaled from 130nm to 90nm which caused decrease in stability.

Shruti H. Choudhari et.al. [3] proposed design and simulated different topologies of SRAM cell. They analysed the leakage power. A Cadence device was used to implement the gpdk 90nm innovation library. SRAM gives a 40–60% decrease in leakage power consumption considering a power supply voltage of 1 V and a 10–20% abatement in read and compose delays. The planned strategies and leakage estimates of various topologies shows that MT-CMOS are better than different topologies.

Shilpi Birla et.al. [4] proposed design and performance of an 8-transistor FinFET SRAM bit-cell for low power applications. They concluded that the main problems in this project are reducing SNM and leakage power. The FinFET structure has a number of issues, including leakage power and stability. With the help of SRAM that has been stimulated on 20nm Predictive Technology Model, it shows that leakage power reduces by 29% and improvement by 5% in SNM using an Low Power Insulated Gate mode with a voltage of 0.5V-1V in circuit. With this, we can get better stability of 5% and leakage power of 29%. It provides a low voltage of LP-IG at 0.2v.

Aswathy A Kumar et.al. [5] proposed the design and analysis of a 6-transistor SRAM cell based on planar and non-planar technology. During the CMOS device when scaling is reduced, problems arises, such as SCE. As a result, FinFET technology is used. SNM is observed for write margin, read current, and leakage by plotting butterfly curve. It provides more stability for DC SNM than planar SRAM for all temperatures. Non-planar SRAM gives reduced leakage and consumption of power than planar SRAM for all the read current and provides greater speed of read operation. Hence, it reduces leakage current and read current for all temperatures.

Vijayalakshmi et.al. [6] proposed the design and modelling of an 18nm 6T FinFET SRAM and analysed the characteristics of these cells in terms of average power and temperature. SRAM is designed and stimulated with the help of a cadence virtuoso tool using 18nm FinFET technology. Power consumption is the main issue in CMOS technology, so we use a multi-gate device. With the Cadence Virtuoso tool, Cadence reduced the average power and temperature of the 6-transistor FinFET SRAM cell in 18nm technology. The average power and the temperature utilized by the circuit is 121 nW and 125°C respectively.

Rajeev Ratna Vallabhuni et.al. [7] proposed the design of a 6-transistor SRAM cell by 18nm Fin Field Effect Transistor technology and 180nm MOSFET technology. They noted that power dissipation was increasing and a decrease in the propagation delay when the voltage was raised from 0 V-1 V in 18nm FinFET technology. In 18nm FinFET technology, the delay is reduced by 90% compared to MOSFET technology. They also implemented area for both MOSFET and FinFET technology and observed that the area of 6-transistor SRAM MOSFET has taken 95um², while the 6-transistor SRAM FinFET has taken 1.37um². This shows that FinFET technology is better than MOSFET technology.

Deepika Sharma et.al. [8] developed a novel 10-transistor CMOS and FinFET SRAM cell designed using different technologies (45nm and 32nm). The major requirements of the VLSI are low power and high-performance memories. Problems arises due to CMOS scaling which is solved by FinFET circuits. They analysed different parameters of SRAM such as power, SNM, and delay. The power is reduced around 90% in 45nm and 32nm FinFET than CMOS. Similarly, delay in read and write modes are reduced around 55% and 60% in 45nm and 32nm respectively. HSNM and RSNM values shows an increase in 45nm and 32nm of FinFET SRAM cell compared to CMOS SRAM cell. Read and write The performance is implemented in HSPICE at 0.5V and 25°C.

III. OBJECTIVES
1. To design SRAM Cell using CMOS Technology in different topologies and find the delay, power and SNM.
2. To design SRAM Cell using FinFET Technology in different topologies and find the delay, power and SNM.
3. To compare SRAM Cell using CMOS Technology and FinFET Technology for delay, power and SNM.
IV. METHODOLOGY

1. METHODOLOGY 1

Fig. 1: Flow Chart for different SRAM cell topologies using (45nm and 90nm) CMOS technology to find read delay, write delay and SNM.

- From Fig. 1, the proposed design will start by creating a new library in Cadence Virtuoso.
- Inside the project library, create a new schematic for designing the SRAM Cell.
- Design the SRAM cell by using different topologies (4T, 6T, 9T, and 14T) in the schematic window.
- Creating the test bench for each topology to analyse delay and power.
- Attaching the 45nm and 90nm CMOS technology model library files in setup.
- Simulating different SRAM cell topologies to test their functionality on a test bench.
- Calculate the read delay, write delay, and power by using the calculator tool.
- Finding HSNM, RSNM, and WSNM by using the Butterfly curve method.

2. METHODOLOGY 2

Fig. 2: Flow Chart for different SRAM cell topologies using (7nm and 16nm) FinFET technology to find read delay, write delay and SNM.

- From Fig. 2, the proposed design will start by creating a new library in Cadence Virtuoso.
- Inside the project library, create a new schematic for designing the SRAM Cell.
- Design the SRAM cell by using different topologies (4T, 6T, 9T, and 14T) in the schematic window.
- Creating the test bench for each topology to analyse delay and power.
- Attaching the 7nm and 16nm FinFET technology (PTM-MG) model library files in setup.
- Simulating different SRAM cell topologies to test their functionality on a test bench.
- Calculate the read delay, write delay, and power by using the calculator tool.
- Finding HSNM, RSNM, and WSNM by using the Butterfly curve method.
3. METHODOLOGY

- After the schematic, tabulate the values of delay and power of different topologies of CMOS based SRAM cells.
- Tabulate all the three SNM values by plotting the Butterfly curve of different topologies of CMOS based SRAM cells.
- Similarly, tabulate the values of delay and power of different topologies of FinFET based SRAM cells.
- Tabulate all the three SNM values by plotting the Butterfly curve of different topologies of FinFET based SRAM cells.
- Compare the tabulated values of both technologies based on delay, power, and SNM.

IV. PROPOSED WORK

![Fig. 3: 9T SRAM Schematic Using 45nm CMOS Technology](image)

Fig. 3 shows the schematic of the 9T SRAM using 45nm CMOS technology in the Cadence Virtuoso Tool. This 9T SRAM design consists of 9 transistors, 2 PMOS and 7 NMOS.

For read operation, BL and BL_Bar act as output. This operation makes WL input and RWL input as high. Here, the 9T CMOS SRAM read the inputs of Q and Q_Bar stored data as low or high.

For write operation, BL and BL_Bar act as input. WL input is always high for write operation. Here, 9T CMOS SRAM will write the inputs of Q and Q_Bar stored data as low or high.

![Fig. 4: 9T SRAM Schematic Using 7nm FinFET Technology](image)

To succeed the limitations of CMOS technology, 7nm FinFET spectra models are used. Fig. 4 shows the schematic of the 9T SRAM using 7nm FinFET Technology in the Cadence Virtuoso Tool.

For read operation, BL and BL_Bar act as outputs. This operation makes WL input and RWL input as high. Here, the 9T FinFET SRAM read the inputs of Q and Q_Bar stored data as low or high.

For write operation, BL and BL_Bar act as inputs. WL input is always high for write operation. Here, 9T FinFET SRAM will write the inputs of Q and Q.Bar stored data as low or high.
Fig. 5: SNM Schematic of 9T SRAM Using 45nm CMOS Technology

Fig. 5 shows the SNM Schematic of 9T SRAM using 45nm CMOS Technology in the Cadence Virtuoso Tool. To find the SNM, a $V_{dc}$ is applied to Q and the output is viewed in $Q_{\text{Bar}}$.

Fig. 6: SNM Schematic of 9T SRAM Using 7nm FinFET Technology

To succeed the limitations of CMOS technology, 7nm FinFET spectra models are used. Fig. 6 shows the SNM Schematic of 9T SRAM using 7nm FinFET Technology in the Cadence Virtuoso Tool. To find the SNM, a $V_{dc}$ is given to Q and the output is viewed in $Q_{\text{Bar}}$.

For the Hold SNM operation, all inputs are low. The HSNM is calculated by analysing the voltage transfer characteristics (VTC) of each half-cell, plotting a butterfly curve.

For the Read SNM operation, all inputs are high. It prevents SRAM cell from inverting the stored value. The value of Read SNM is least, means it is extremely vulnerable.

For the write SNM operation, BL and WL inputs are high, and BLB and RWL are low. WSNM is defined as minimum bit line required to invert the state of a cell. WSNM is defined as the width of the smallest square that can be built-in between the lower-right half of the curve, means between Write Voltage Transfer Characteristic (WVTC) and Read Voltage Transfer Characteristic (RVTC).

Similarly, other topology schematics for 45nm CMOS and 7nm FinFET technologies are done, and also for 90nm CMOS and 16nm FinFET technologies.
V. STIMULATED WAVEFORMS AND RESULTS

Fig. 7: Transient response for the read operation of 9T SRAM using 45nm CMOS technology

Fig. 8: Transient response for the write operation of 9T SRAM using 45nm CMOS technology

Fig. 7 and Fig. 8 depict the transient response performed for the read operation and write operation of 9T SRAM using 45nm CMOS Technology, respectively.

Fig. 9: Transient response for the read operation of 9T SRAM using 7nm FinFET technology

Fig. 10: Transient response for the write operation of 9T SRAM using 7nm FinFET technology

Fig. 9 and Fig. 10 depict the transient response performed for the read operation and write operation of 9T SRAM using 7nm FinFET Technology, respectively.
Fig. 11: Hold SNM, Read SNM and Write SNM Butterfly curves of 9T SRAM using 45nm CMOS technology

Fig. 12: Hold SNM, Read SNM and Write SNM Butterfly curves of 9T SRAM using 7nm FinFET technology

Fig. 11 and Fig. 12 depict the SNM Butterfly curves of Hold, Read and Write of 9T SRAM using 45nm CMOS and 7nm FinFET technologies, respectively.

**SNM calculation**

SNM = “Maximum Side of the Square” = Maximum diagonal length of Square / √2

Similarly, we have analysed other topology parameters like read and write delay, power and SNM Butterfly curves for 45nm CMOS and 7nm FinFET technologies, and also for 90nm CMOS and 16nm FinFET technologies.
TABLE I. Results of various parameters for (45nm and 90nm) CMOS and (7nm and 16nm) FinFET technology in various topologies.

<table>
<thead>
<tr>
<th>Topology</th>
<th>Parameters</th>
<th>CMOS (45nm)</th>
<th>CMOS (90nm)</th>
<th>FinFET (7nm)</th>
<th>FinFET (16nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Read Delay</td>
<td>119.5p</td>
<td>147.1p</td>
<td>96.61f</td>
<td>245.2f</td>
</tr>
<tr>
<td></td>
<td>Write Delay</td>
<td>319.0p</td>
<td>330.2p</td>
<td>290.0p</td>
<td>249.7p</td>
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<tr>
<td>4T</td>
<td>Power</td>
<td>11.88u</td>
<td>33.9u</td>
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<tr>
<td></td>
<td>HSNM</td>
<td>173mV</td>
<td>226mV</td>
<td>125mV</td>
<td>160mV</td>
</tr>
<tr>
<td></td>
<td>RSNM</td>
<td>121mV</td>
<td>182mV</td>
<td>24mV</td>
<td>49mV</td>
</tr>
<tr>
<td></td>
<td>WSNM</td>
<td>231mV</td>
<td>342mV</td>
<td>164mV</td>
<td>203mV</td>
</tr>
<tr>
<td></td>
<td>Read Delay</td>
<td>119.7p</td>
<td>149.5p</td>
<td>96.53f</td>
<td>249.6f</td>
</tr>
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<td>Write Delay</td>
<td>356.4p</td>
<td>741.2p</td>
<td>188.6p</td>
<td>308.1p</td>
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<tr>
<td>6T</td>
<td>Power</td>
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<td>9.363u</td>
<td>486.9n</td>
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<tr>
<td></td>
<td>HSNM</td>
<td>245mV</td>
<td>282mV</td>
<td>155mV</td>
<td>184mV</td>
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<tr>
<td></td>
<td>RSNM</td>
<td>158mV</td>
<td>210mV</td>
<td>78mV</td>
<td>104mV</td>
</tr>
<tr>
<td></td>
<td>WSNM</td>
<td>289mV</td>
<td>400mV</td>
<td>190mV</td>
<td>212mV</td>
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<tr>
<td></td>
<td>Read Delay</td>
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<td>147.4p</td>
<td>99.01f</td>
<td>245.6f</td>
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<tr>
<td></td>
<td>Write Delay</td>
<td>367.0p</td>
<td>761.6p</td>
<td>340.0p</td>
<td>352.4p</td>
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<tr>
<td>9T</td>
<td>Power</td>
<td>599.0n</td>
<td>10.44u</td>
<td>500.2n</td>
<td>580.4n</td>
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<tr>
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<td>252mV</td>
<td>286mV</td>
<td>159mV</td>
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<tr>
<td></td>
<td>RSNM</td>
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<td>248mV</td>
<td>103mV</td>
<td>132mV</td>
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<tr>
<td></td>
<td>WSNM</td>
<td>295mV</td>
<td>410mV</td>
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<tr>
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<td>Write Delay</td>
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<td>14T</td>
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<td>288mV</td>
<td>161mV</td>
<td>193mV</td>
</tr>
<tr>
<td></td>
<td>RSNM</td>
<td>156mV</td>
<td>215mV</td>
<td>72mV</td>
<td>97mV</td>
</tr>
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<td>WSNM</td>
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<td>250mV</td>
<td>292mV</td>
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</table>

Table 1 shows the results of read delay, write delay, power and SNM (HSNM, RSNM, WSNM) for (45nm and 90nm) CMOS technology and (7nm and 16nm) FinFET technology in various topologies. From these results, FinFET SRAM shows better performance than CMOS SRAM.

VI. CONCLUSION

The project work carried out has generated useful conclusions. The different topologies of SRAM cells are designed. The parameters like delay, power, and SNM for each topology are calculated and analysed using 45nm and 90nm CMOS technology. The simulation results of the same have been analysed for 7nm and 16nm PTM-MG FinFET technology. All these results are generated by Cadence Virtuoso Software. The designed SRAM Cell at 7nm and 16nm PTM-MG FinFET Technology outperforms 45nm CMOS Technology in terms of delay, power, and SNM. If a processor has to have a fast working cache memory, then FinFET SRAM cell is best in comparison with CMOS SRAM cell. And likewise, in a different application where certain parameters in which CMOS SRAM cell are vulnerable, in those situations FinFET SRAM cell excels over CMOS SRAM cell. The outcomes appear to show that FinFET based SRAM is quicker, dependable, and the force utilization is fundamentally decreased and offers great exchange at lower technology nodes.

REFERENCES


