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LOW POWER 4×1 MULTIPLEXER DESIGN USING CMOS AND FINFET TECHNOLOGIES

S.J.V.Sravani[1], R.Lokesh[1], Y.K.V.S.D.Naveen[1], Y.D.Shankar[1], T.S.S.Kiran Kumar[1], I. Rama Satya Nageswara Rao[2], Kondamuri Naga Teja[2]

[1]UG Scholar, Department of Electronics and Communication Engineering, Bonam Venkata Chalamayya Engineering College,Odalarevu, Andhra Pradesh, India

[2]Assistant Professor, Department of Electronics and Communication Engineering, Bonam Venkata Chalamayya Engineering College,Odalarevu, Andhra Pradesh, India

Abstract

Low power digital circuit design is a major challenge in modern Very Large Scale Integration (VLSI) systems. Multiplexers are fundamental components widely used in communication systems, processors, and data routing circuits. This paper presents the design and simulation of a low power 4×1 multiplexer implemented using conventional CMOS technology and advanced FinFET technology. The proposed designs are analyzed using DSCH and Microwind simulation tools. Performance metrics such as power consumption, propagation delay, area utilization, and power delay product are evaluated. Simulation results show that the FinFET based multiplexer significantly reduces power consumption and delay compared with CMOS based implementation. The results demonstrate the suitability of FinFET technology for future nanoscale VLSI circuits.

Keywords

Multiplexer, CMOS, FinFET, Low Power VLSI, Microwind, DSCH, Nanoelectronics

1. Introduction

The rapid growth of portable electronic devices such as smartphones, wearable systems, and IoT devices has increased the demand for energy efficient digital circuits. Multiplexers are widely used in digital communication systems, microprocessors, memory circuits, and signal routing applications. Conventional CMOS technology has been the dominant technology for digital integrated circuits for several decades. However, aggressive technology scaling has introduced several issues such as leakage currents, short channel effects, and increased power dissipation. FinFET technology has emerged as a promising solution to overcome these limitations. FinFET devices utilize a three dimensional gate structure that provides better electrostatic control over the channel, resulting in reduced leakage current and improved switching performance.

2. Multiplexer Architecture

A 4×1 multiplexer consists of four input lines, two selection lines, and one output line. The selection inputs determine which input signal is transmitted to the output. The logical expression for the output of a 4×1 multiplexer is given by:

$$Y = D0\ S1'\ S0' + D1\ S1'\ S0 + D2\ S1\ S0' + D3\ S1\ S0$$

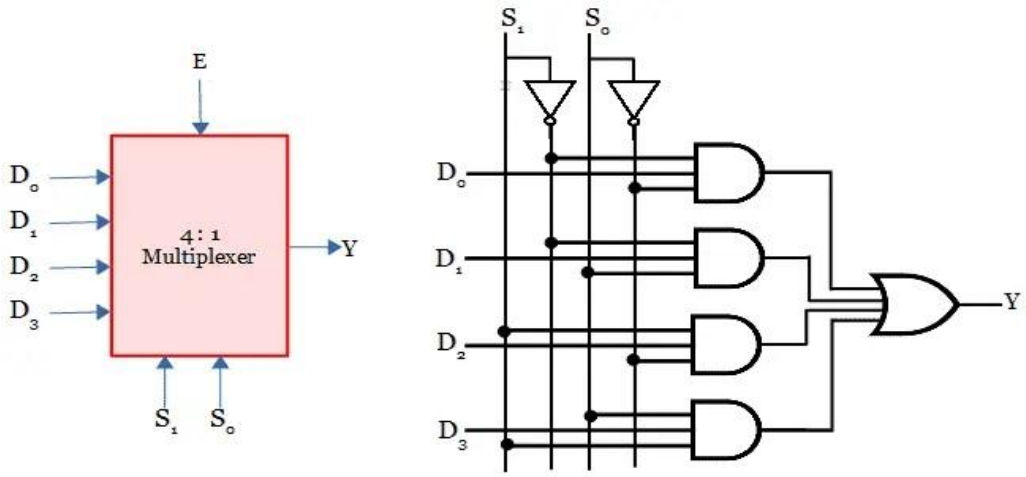


Fig.1 Block diagram of 4×1 multiplexer

3. CMOS Implementation

The CMOS implementation of the multiplexer uses complementary PMOS and NMOS transistors to implement the required logic functions. CMOS circuits offer advantages such as high noise immunity and low static power consumption. However, as technology scales below 45 nm, leakage currents and short channel effects become significant challenges.

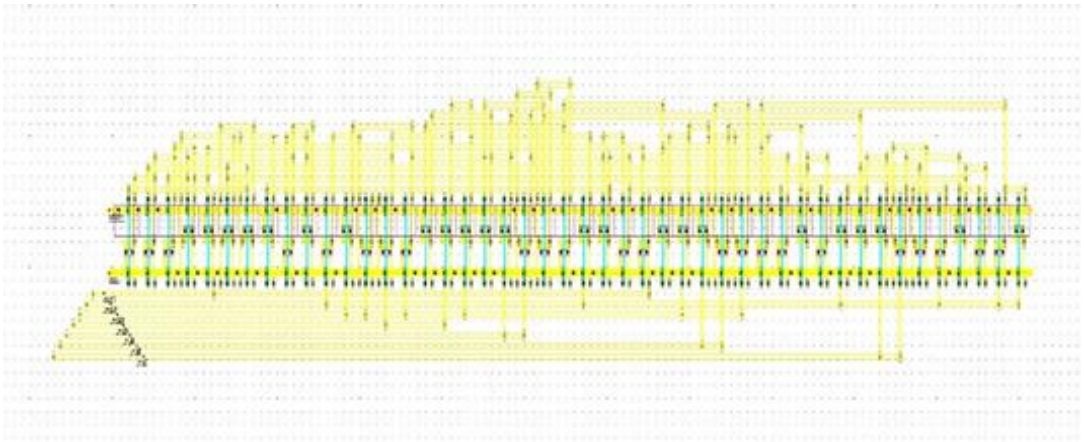


Fig.2 Conceptual CMOS layout structure

4. FinFET Based Design

FinFET devices are multi gate transistors where the channel is formed in a thin silicon fin. The gate wraps around the channel providing superior control over carrier transport. FinFETs significantly reduce leakage current and improve drive current compared to planar MOSFET devices.

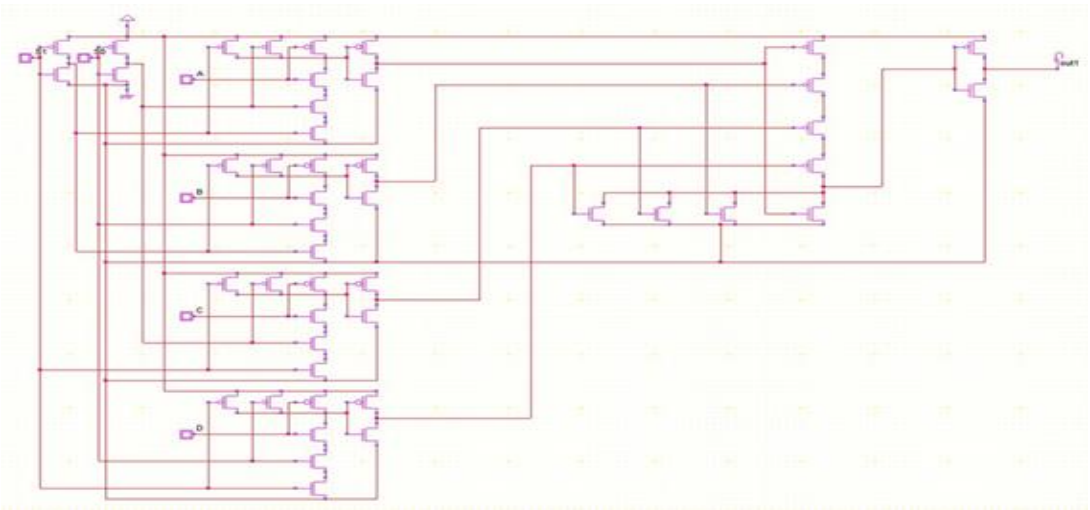


Fig.3 FinFET device structure

5. Simulation Methodology

The multiplexer circuits were designed using DSCH schematic editor and implemented in Microwind layout environment. CMOS implementation used 45 nm technology parameters while FinFET implementation used 7 nm device parameters. Transient simulations were performed to verify functional correctness and evaluate performance metrics.

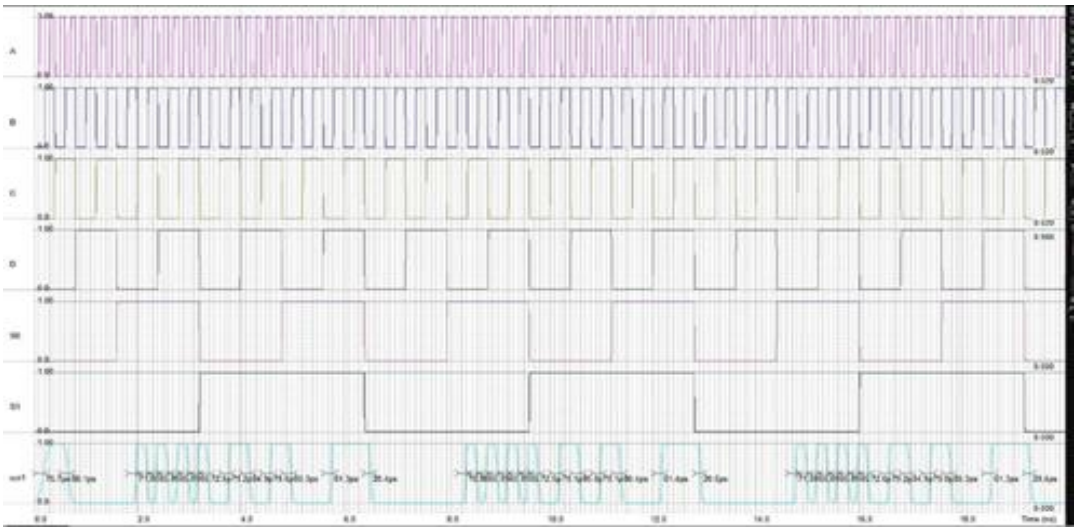


Fig.4 Simulated input and output waveforms

6. Results and Performance Analysis

Simulation results demonstrate significant improvement in performance when using FinFET technology. Power consumption is reduced by nearly 90 percent compared to CMOS implementation. Propagation delay is also significantly reduced due to improved carrier transport properties of FinFET devices.

Parameter	CMOS 45 nm	FinFET 7 nm
Power Consumption	46.551 µW	3.837 µW
Propagation Delay	82.05 ps	27 ps
Area	158.9 µm²	4.0 µm²
Power Delay Product	3.819×10^{-15}	0.103×10^{-15}

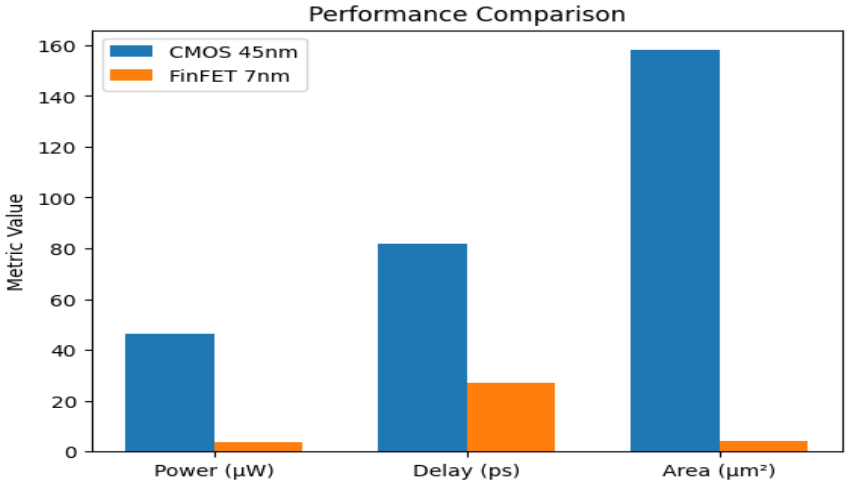


Fig.5 Performance comparison between CMOS and FinFET designs

7. Conclusion

This paper presented the design and analysis of a low power 4×1 multiplexer using CMOS and FinFET technologies. Simulation results confirm that FinFET based design achieves lower power consumption, reduced delay, and smaller area compared with conventional CMOS implementation. The proposed approach can be extended to larger multiplexers and complex digital circuits in future nanoscale VLSI systems.

References

[1] D. J. Frank *et al*., "Device scaling limits of Si MOSFETs," *Proceedings of the IEEE*, vol. 89, no. 3, pp. 259–288, Mar. 2001.
[2] M. Alioto, *Ultra Low Power VLSI Circuit Design*. New York, NY, USA: Springer, 2012.
[3] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge, U.K.: Cambridge University Press, 1998.
[4] S. Borkar, "Design challenges of technology scaling," *IEEE Micro*, vol. 19, no. 4, pp. 23–29, Jul./Aug. 1999.
[5] E. Sicard and S. Delmas-Bendhia, *Microwind and DSCH VLSI Design Tools*. Boston, MA, USA: Springer, 2007.
[6] J.-P. Colinge, *FinFETs and Other Multi-Gate Transistors*. New York, NY, USA: Springer, 2008.
[7] International Technology Roadmap for Semiconductors (ITRS), "International technology roadmap for semiconductors," 2015.
[8] N. H. E. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed. Boston, MA, USA: Addison-Wesley, 2011.
[9] J. M. Rabaey, A. Chandrakasan, and B. Nikolić, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, NJ, USA: Prentice Hall, 2003.
[10] A. P. Chandrakasan and R. W. Brodersen, "Low-power CMOS digital design," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 4, pp. 473–484, Apr. 1992.