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Design of a Low-Power Redundant Transition-Free TSPC Dual-Edge-Triggering Flip-Flop with a Single-Transistor-Clocked Buffer

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ABSTRACT

In the modern graphics processing unit (GPU)/artificial intelligence (AI) era, flip-flop (FF) has become one of the most power-hungry blocks in processors. To address this issue, a novel single phase-clock dual-edge-triggering (DET) FF using a single-transistor clocked (STC) buffer (STCB) is proposed. The STCB uses a single clocked transistor in the data sampling path, which completely removes clock redundant transitions (RTs) and internal RTs that exist in other DET designs. When operating at switching activity, the proposed STC-DET outperforms prior state-of the-art low power DET in power consumption. It also achieves the lowest power delay-product (PDP) among the DETs using LECTOR Technique to reduce power consumption.

Keywords: Dual edge triggering (DET), Dynamic power, Flip-Flop, LECTOR.

I. INTRODUCTION

Especially in light of the pressure from current graphics processing unit (GPU)/artificial intelligence (AI) neural network processors, power consumption has emerged as one of the top problems for CMOS digital designers. Every 3.4 months, the amount of processing power utilized to train AI doubles [1]. In a contemporary processor, the clocking system can use up to 50% of the overall power [2]. Thus, one of the primary elements to resolving the power dissipation issue noted above has been seen as its power optimization. The two primary components of a processor's clocking system are flip-flops (FFs) and clock distribution networks. Traditional single-phase-clock FFs only process one clock edge at a time to process incoming data, which consumes extra power data processing not yet developed. In order to process data, dual edge triggering (DET) FFs use both clock edges. This allows them to reduce the clock frequency to half while still retaining the same throughput. A flip-flop is a fundamental building block in digital electronics and computer architecture. It is a sequential logic circuit that can store and transfer binary information. Flip-flops are used to create memory elements, registers, counters, and other sequential logic circuits. A flip-flop operates on clock pulses, which are regular signals that synchronize the operation of digital circuits. The clock signal determines when the flip-flop will store or transfer data. The two most common types of flip-flops are the SR (Set-Reset) flip-flop and the D (Data) flip-flop.

II. LITERATURE REVIEW

J. Tschanz, S. Narendra, Zhanping Chen, S. Borkar, M. Sachdev and Vivek De, "Comparative delay and energy of single edge-triggered and dual edge triggered pulsed flip-flops for high-performance microprocessors," ISLPED'01: Proceedings of the 2001 International Symposium on Low Power Electronics and Design (IEEE Cat. No.01TH8581), Huntington Beach, CA, USA, 2001, pp. 147-152 Flip-flops and latches are crucial elements of a design from both a delay and energy standpoint. We compare several styles of single edge-triggered flip-flops, including semi dynamic and static with both implicit and explicit pulse generation. We present an implicit-pulsed, semi dynamic flip-flop (ip-DCO) which has the fastest delay of any flip-flop considered, along with a large amount of negative setup time. However, an explicit-pulsed static flip-flop (ep-SFF) is the most energy efficient and is ideal for the majority of critical paths in the design. In order to further reduce the power consumption, dual edge-triggered flip-flops are evaluated. It is shown that classic dual edge-triggered designs suffer from a large area penalty and reduced performance, prohibiting their use in critical paths. A new explicit pulsed dual edge-triggered flip-flop is presented which provides the same performance as the single edge-triggered version with significantly less energy consumption in the flip-flop as well as in the clock distribution network. Y. Lee, G. Shin and Y. Lee, "A Fully Static True-Single-Phase-Clocked Dual Edge-Triggered Flip-Flop for Near-Threshold Voltage Operation in IoT Applications," in IEEE Access, vol. 8, pp. 40232-40245, 2020 A Dual-Edge-Triggered (DET) flip-flop (FF) that can reliably operate at low voltage is proposed in this paper. Unlike the conventional Single-Edge-Triggered (SET) flip-flops, DET-FFs can improve energy efficiency by latching input data at both clock edges. When combined with aggressive voltage scaling, significant efficiency improvement is expected. However, prior DET-FF designs were susceptible to Process, Voltage and Temperature (PVT) variations, limiting their operation at low voltage regimes. A fully static true-single-phase-clocked DET-FF is 8 proposed to achieve reliable operation at voltages as low as a near-threshold regime. Instead of the two-phase or pulsed clocking scheme in conventional DET-FFs, a True-Single-Phase-Clocking (TSPC) scheme is adopted to overcome clock overlap issues and enable low-power operation. Fully static implementation also enables robust operation in a low voltage regime. The proposed DET-FF is designed in 28nm CMOS technology, and a comprehensive analysis including post-layout Monte Carlo simulation for wide PVT ranges is performed to validate the design approaches. Extensive analysis and comparison with prior-art DET-FFs confirmed that the proposed DET-FF can operate at the lowest voltage of 0.28 V for a temperature range of -40 °C to 120 °C while maintaining nearly-best energy efficiency and power-delay-product.

III. IMPLEMENTATION

In CMOS circuits, the reduction of the threshold voltage due to voltage scaling leads to increase in subthreshold leakage current and hence static power dissipation. We propose a novel technique called LECTOR for designing CMOS gates which significantly cuts down the leakage current without increasing the dynamic power dissipation. In the proposed technique, we introduce two leakage control transistors (a p-type and a n-type) within the logic gate for which the gate terminal of each leakage control transistor

(LCT) is controlled by the source of the other. In this arrangement, one of the LCTs is always "near its cutoff voltage" for any input combination. This increases the resistance of the path from V/sub dd/ to ground, leading to significant decrease in leakage currents. The gate-level netlist of the given circuit is first converted into a static CMOS complex gate implementation and then LCTs are introduced to obtain a leakage-controlled circuit. The significant feature of LECTOR is that it works effectively in both active and idle states of the circuit, resulting in better leakage reduction compared to other techniques. In CMOS circuits, the reduction in threshold voltage resulting from voltage scaling contributes to an increase in subthreshold leakage current, leading to higher static power dissipation. Our proposed approach, named LECTOR, presents an innovative method for designing CMOS gates that markedly reduces leakage current without elevating dynamic power dissipation. The key aspect of this technique involves introducing two leakage control transistors (one p-type and one n-type) within the logic gate, where the gate terminal of each leakage control transistor (LCT) is regulated by the source of the other. This configuration ensures that one of the LCTs is consistently "near its cutoff voltage" for any input combination. Consequently, this increases the resistance along the path from V/sub dd/ to ground, resulting in a substantial decrease in leakage currents. The process involves converting the gate level netlist of the given circuit into a static CMOS complex gate implementation, followed by the introduction of LCTs to achieve a leakage-controlled circuit. 17 Notably, LECTOR effectively operates in both active and idle states of the circuit, delivering superior leakage reduction compared to alternative techniques.

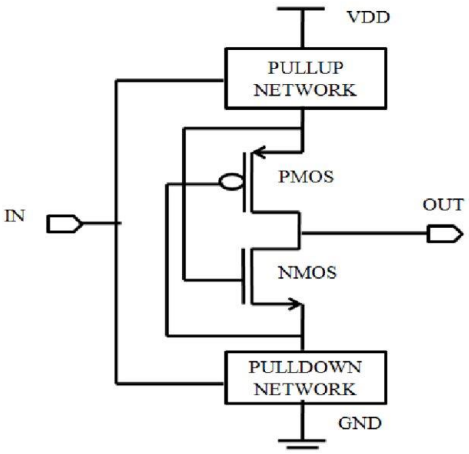

Fig 1: Schematic of LECTOR

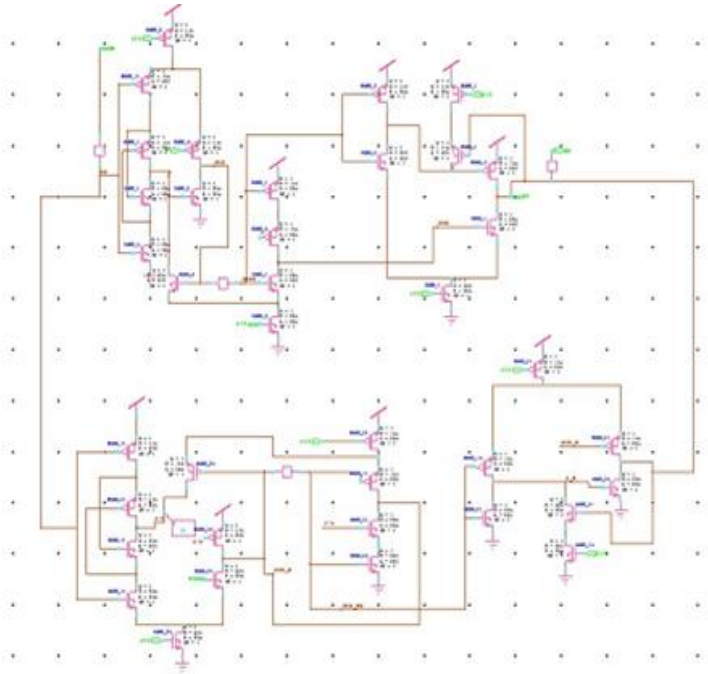

Fig 2: Schematic For STCDET Using LECTOR

A. Operation of the Top FF in STC-DET:

when CLK = 0, and transistors (P2, N2) become equivalent to a virtual inverter [A simplified logic diagram is shown in Fig. 3(a)]. When CLK = 0, the top master latch's clocked PMOS P3 turns on, changing node X to D ″. In contrast, in the top slave latch in Fig. 3, clocked NMOS N4 is off because CLK = 0, therefore node Y will not be 0, thus PMOS P8 is off. The input then travels to MID in the top master latch (see arrow in the upper left of the previous picture). VDD and QT cannot connect or GND, which denotes that the top FF's QT is floating (see the top left of Fig. 3(a)).

A negative-triggered STCB is constructed in Fig by transistors N1, N2, P1, P2, and P3, with the sole timed transistor P3 serving as the signal sampling channel. In contrast to FN_C DET and FS-TSPC, STCDET does not have the RT that exists between a clocking PMOS and a clocking NMOS. No argument exists either. A second clock-driven NMOS transistor, N3, is present in the top master latch (top left of Fig.3), although it is employed in the keeper rather than the data sampling path. It is clocked similarly to transistor P3. The four transistors that are clocking together are all on the data sampling path have been marked out with an arrow in Fig.4 (P3, N4, N5, and P6). Transistors (N4, N7, N8, P7, P8) build another positive triggered STCB in the top FF.

When CLK = 1, the routes connected to P1 and consequently N2 in the top master latch of Fig. 4 are off because clocked PMOS P3 is off because CLK = 1. The logic state of MID is therefore maintained by keeper (N3, N15, P14, P15). X will be maintained by pull down keeper (N14, N3) while its logic state is 0. The timed NMOS, N4, however, turns on at the top slave latch, making Y be MID″,

which is virtually MID. The signal from MID, which is just before the clock rising edge, travels to QT as a result of transistors (N8, P8) acting as a virtual inverter. as a result, the top FF is activated at the clock positive edge.

B. Operation of the Bottom FF in STC-DET:

The clock NMOS, N5, in the bottom master latch goes off when CLK = 0 in the bottom FF (see bottom left of Fig. 3). As a result, the routes connected to N9 and P10 are inactive, and keeper (N16, N17, P5, P17) maintains the logic state of MID_n. If the logic state of X_n is 1, keeper (P16, P5) will maintain that state. However, in the bottom slave latch (bottom right of Fig. 3), when CLK = 0, the timed PMOS P6 in the top of the figure switches on, transforming Y_n into MID_n, which is essentially MID_n. As a result, P12 and N12 work as a virtual inverter, and the signal of MID_n appears. I D_n, just before the clock falling edge passes to QT (see arrow in left half of Fig. 3(b)), is at this time. As a result, on the clock's negative edge, the bottom FF is engaged.

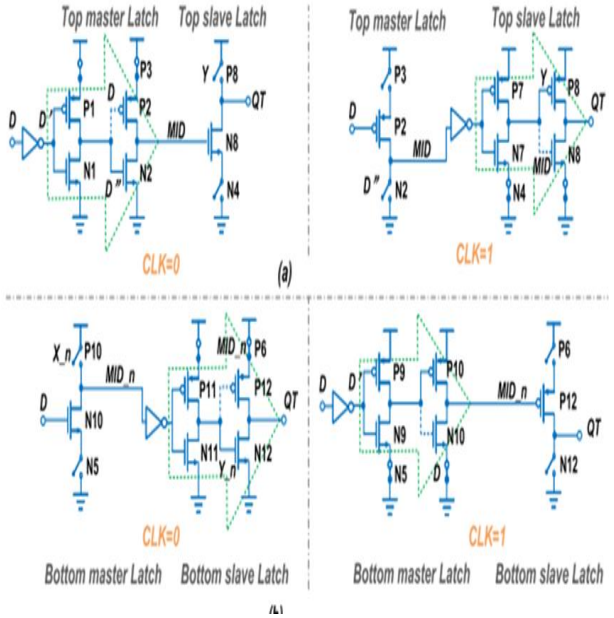

Fig 3: Operation of the proposed STC-DET: (a) Top FF and (b) bottom FF using equivalent simplified logic circuit diagram.

IV. RESULTS AND DISCUSSION

Schematic:

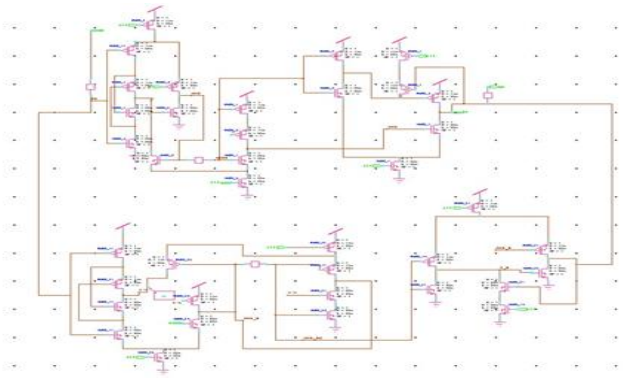

Fig 4: Schematic For STCDET Using LECTOR

Waveform:

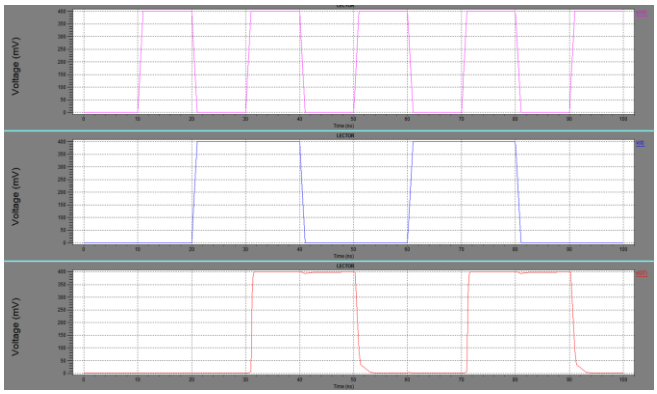

Fig 5: Waveform For STCDET Using LECTOR

Area:

```
Device and node counts:
MOSFETs - 54
   BJTs - 0
MESFETs - 0
```

Power:

```
Power Results
vl from time 0 to 1e-007
Average power consumed -> 1.206081e-007 watts
Max power 1.861622e-006 at time 3.1223e-008
Min power 1.793915e-008 at time 4e-008
```

Delay:

```
delay = 2.0820e-008
   Trigger = 1.0250e-008
   Target  = 3.1070e-008
```

V. CONCLUSION

A unique low-power redundant-transition-free dual-edge-triggered FF is proposed, known as STC-DET, because it makes use of STC buffers to totally eliminate RT in dual-edge-triggered FFs which two The positive-triggered and negative-triggered STC buffers in the topology each have just one timed transistor in the data sampling circuit, eliminating all clock redundant components, transitions and internal redundant transitions that were present in prior DET systems between two clocked transistors. Furthermore, the proposed STC-DET has no controversy. at terms of power dissipation, Additionally, among all DET designs, STC-DET consumes the least amount of power in all process corners at various voltages for switching activity in conclusion, among all the DET FFs of the state-of-the-art, the suggested STC-DET achieves the lowest power consumption in the average switching activity range.but if we use LECTOR approach in STCDET means still power may reduce.

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